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AB35B-A4S

VER 6.0

Model Name: TB350-BTC

2017/03/17

CPU: AMD AM4

System

Chipset: PROM1

Main

Memory: Dual Channel/DDR4

Onboard Device:

Super I/O:IT8613E

LAN : RTL8111H/RTL8106E/8118AS

HD Codec:ALC887 3 jacks

Power solution:

CPU Voltage Regulators:3phase by ISL95712

VDDNB voltage Regulators:2phase by ISL95712

APU_VDDR/P_RUN voltage Regulators:LDO

DDR voltage Regulators:1Phase

Expansion Slots:

PCI EXPRESS 16X SLOT*1

PCI EXPRESS 1X SLOT*5

REAR I/O:

PS/2 KBMS*1

DVI Port*1

2 layer USB3.0*2

2 layer USB2.0 + RJ45 Ports*1

Front I/O:

Audio Jackets 3jets*1

USB3.0 Header*1

SATA3 Connectors*4

USB2.0 Header*2

CPU FAN*1

System1 FAN*1

Serial header*1

Front Audio Header*1

Front Panel Header*1

COLAY AA32B-A4S
TA320-BTC

Features	Family 15h Models 60h-6Fh in AM4 Infrastructure	Family 17h Models 00h-0Fh in AM4 Infrastructure	Family 17h Models 10h-1Fh in AM4 Infrastructure
APU Graphics	OPN Specific	Not Supported	OPN Specific
DDR4	Supported	Supported	Supported
DDR3	Not Supported	Not Supported	Not Supported
DDR3L	Not Supported	Not Supported	Not Supported
DDR3U	Not Supported	Not Supported	Not Supported
SODIMMs	Supported	Supported	Supported
Unbuffered DIMMs	Supported	Supported	Supported
ECC	OPN Specific	OPN Specific	OPN Specific
PCIe® Graphics	Up to 1 x8 Gen3	Up to 1 x16 Gen3 or 2 x8 Gen3	Up to 1 x8 Gen3
PCIe® GPP	Up to 6 x1 Gen3	Up to 8 x1 Gen3 ³	Up to 8 x1 Gen3 ³
Azalia	Supported	Supported	Supported
SATA 3.0	Up to 2 Gen3	Up to 2 Gen3 ³	Up to 2 Gen3 ³
SATA Express	Not Supported	Supported ³	Supported ³
SPI	Supported	Supported	Supported
eSPI	Supported	Supported	Supported
LPC	Supported	Supported	Supported
USB 2.0	Supported	Supported	Supported
Features	Family 15h Models 60h-6Fh in AM4 Infrastructure	Family 17h Models 00h-0Fh in AM4 Infrastructure	Family 17h Models 10h-1Fh in AM4 Infrastructure
USB 3.1	Up to 4 Gen1 ports	Up to 4 Gen1 ports	Up to 3 Gen2 ports and 1 Gen1 port
DDI	Supported	Not Supported	Supported
SVI2 ¹	Supported	Supported	Supported
SB-TSI ²	Supported	Supported	Supported

HW Engineer:

Date:

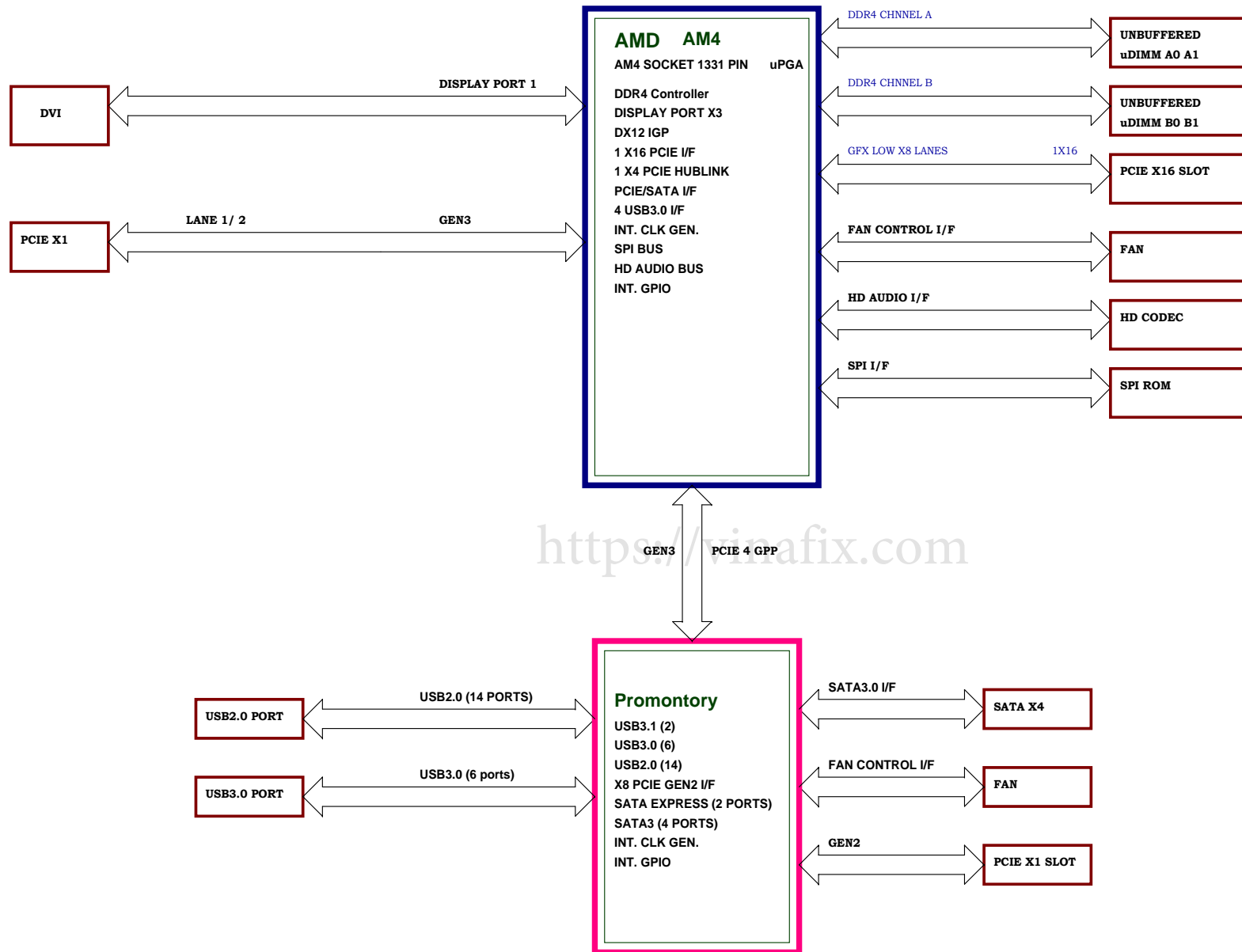
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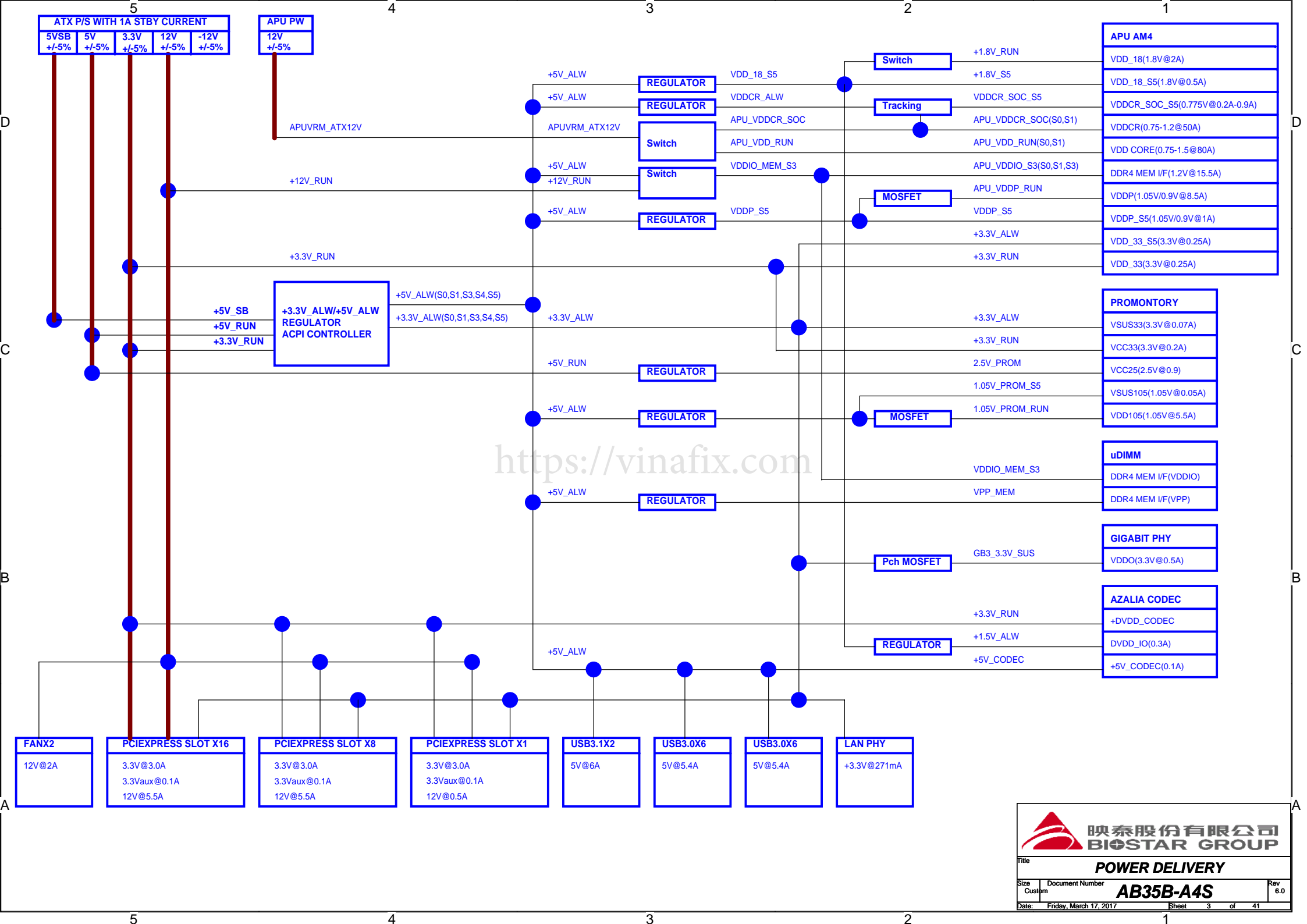
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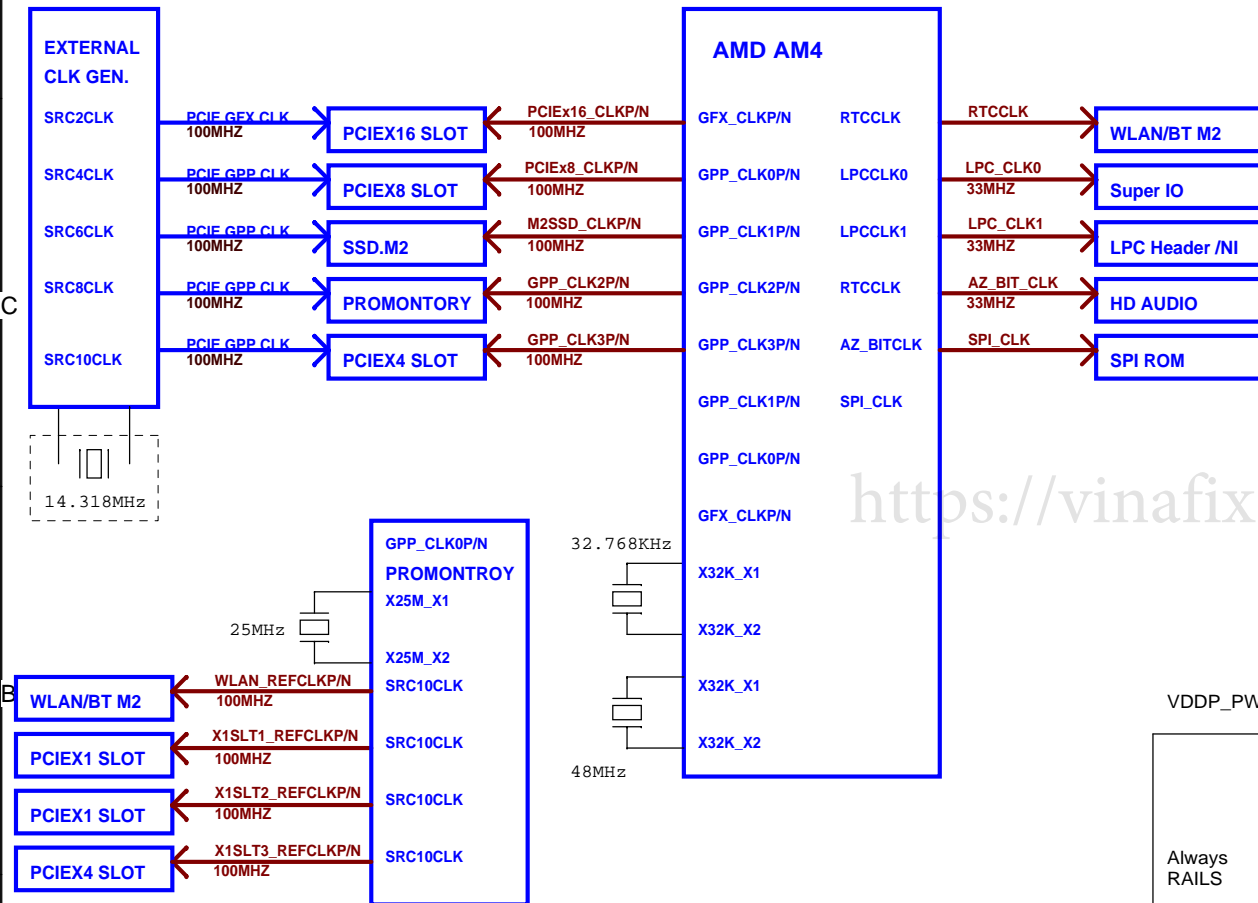
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Title		COVER	
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APU:
1, VDDIO ramp before PCIE_RST#
(VDD_RUN, VDDP,

PWR_GOOD

APU_VDD_RUN_PG

APU_VDD_RUN

APU_VDD_RUN_EN

VDDIO_PWRGD

2.5V_PROM

VDDP

+1.8V/+1.05V

+12V

+5V/+3.3V

PS_ON

SLP_S3#

VPP_PWRGD

VPP_MEM/VTT_MEM

VDDIO_MEM_S3

SLP_S5:

PWR_BTN

RSMRS⁺

VDDP_PWRGD/PM_1V05_PWRGD

1.05V_PROM_S5

VDDP_S

+1.5V_A

VDD_18_S5

+3.3V_ALW(from +3.3VSB)

+5V_ALW(from +5VSB)

+3.3VS

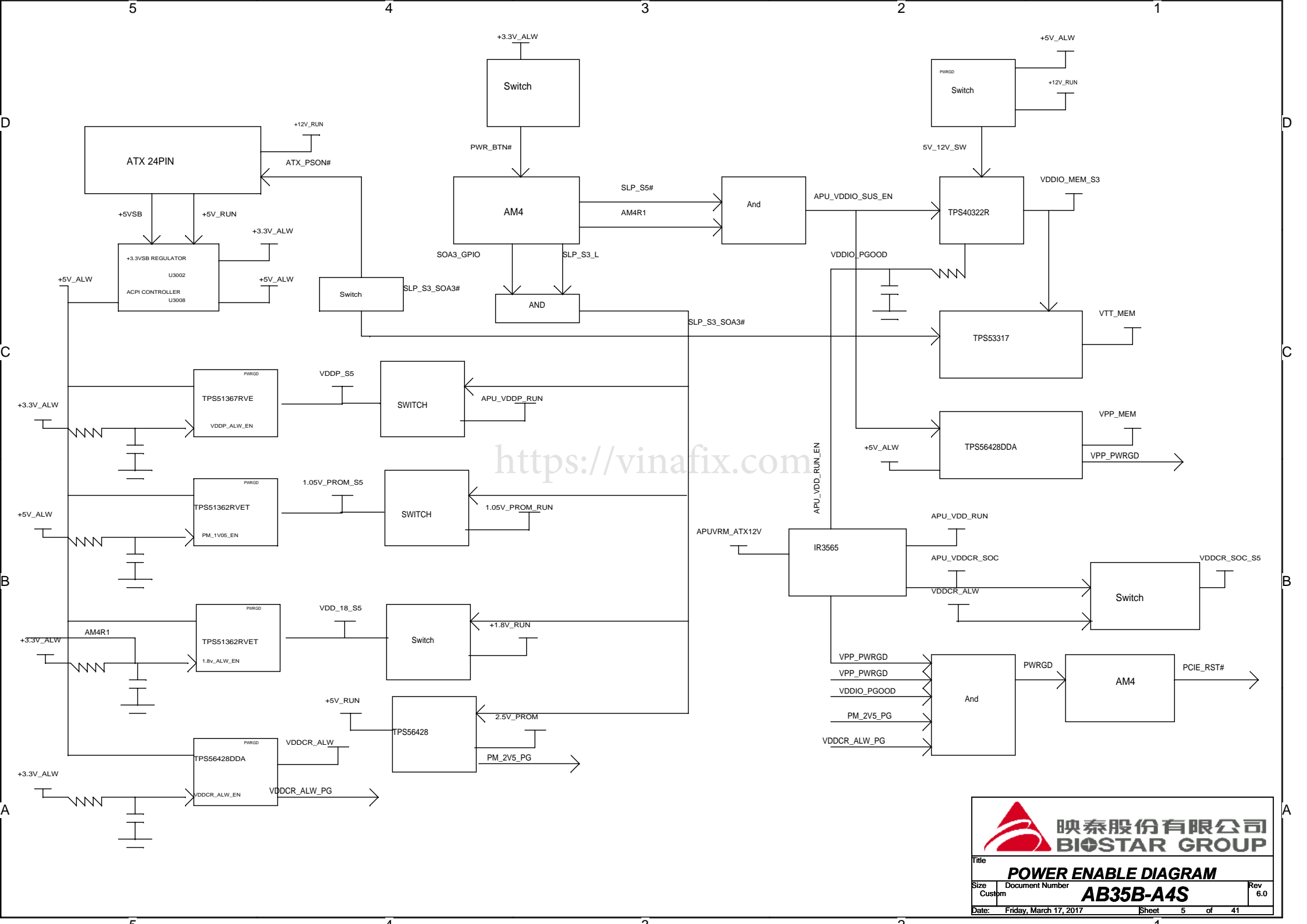
+5VSB

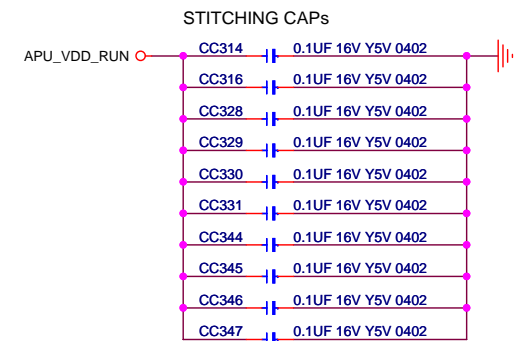
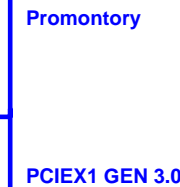


Title	CLOCK/SEQUENCE
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Size Custom	Document Number AB35B-A4S	Rev 6.0
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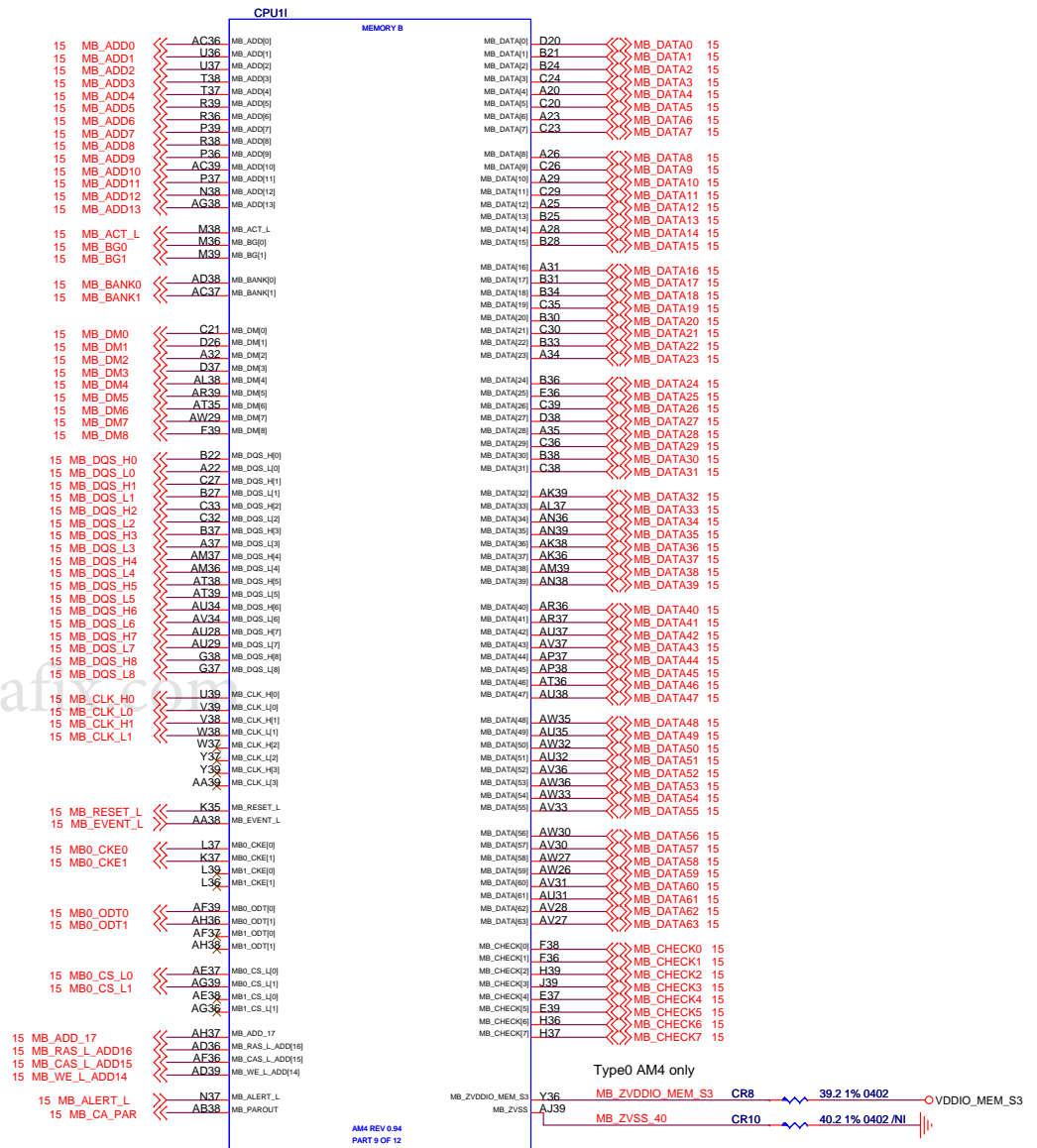
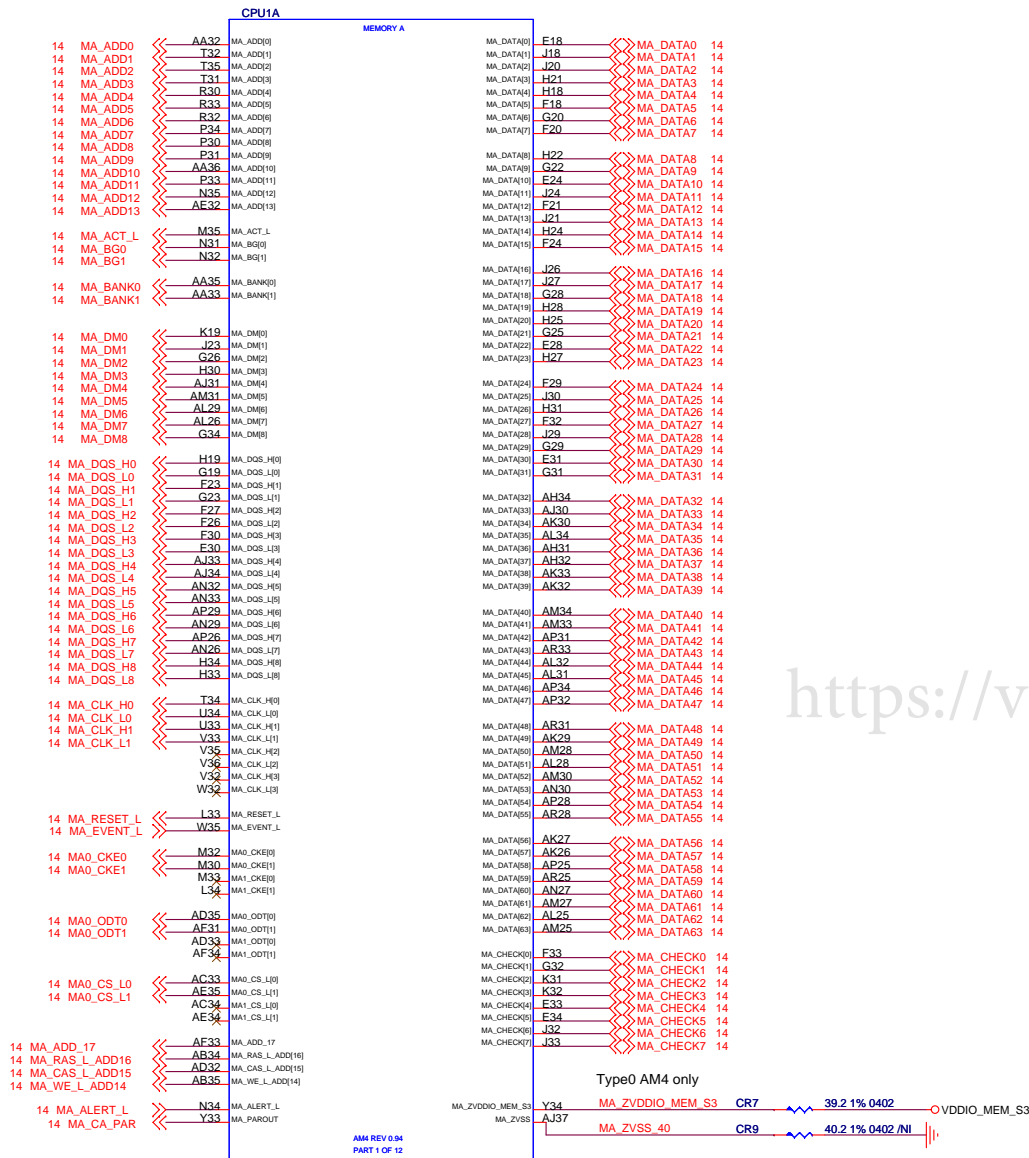


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C

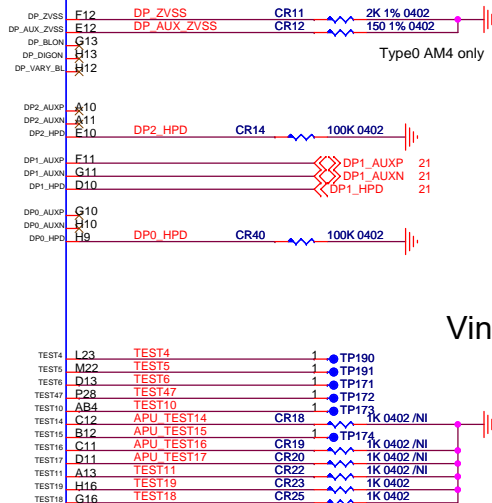
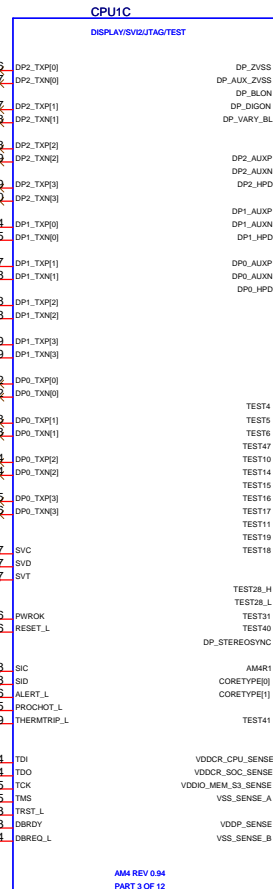
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A

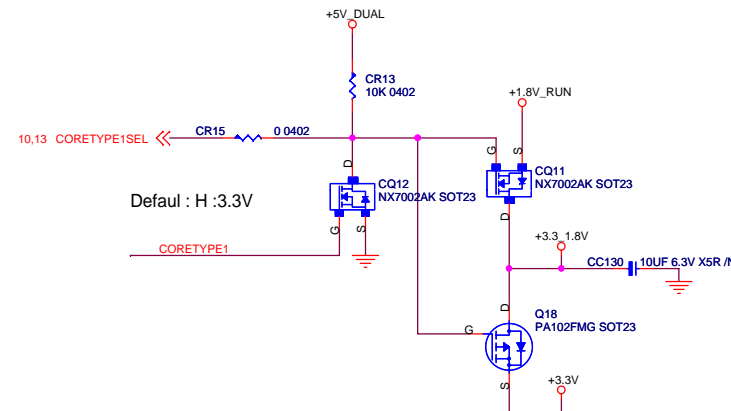


DVI

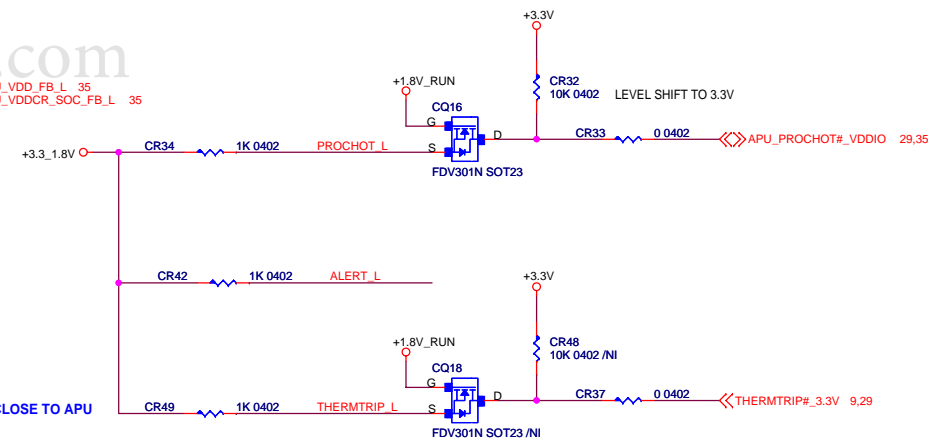
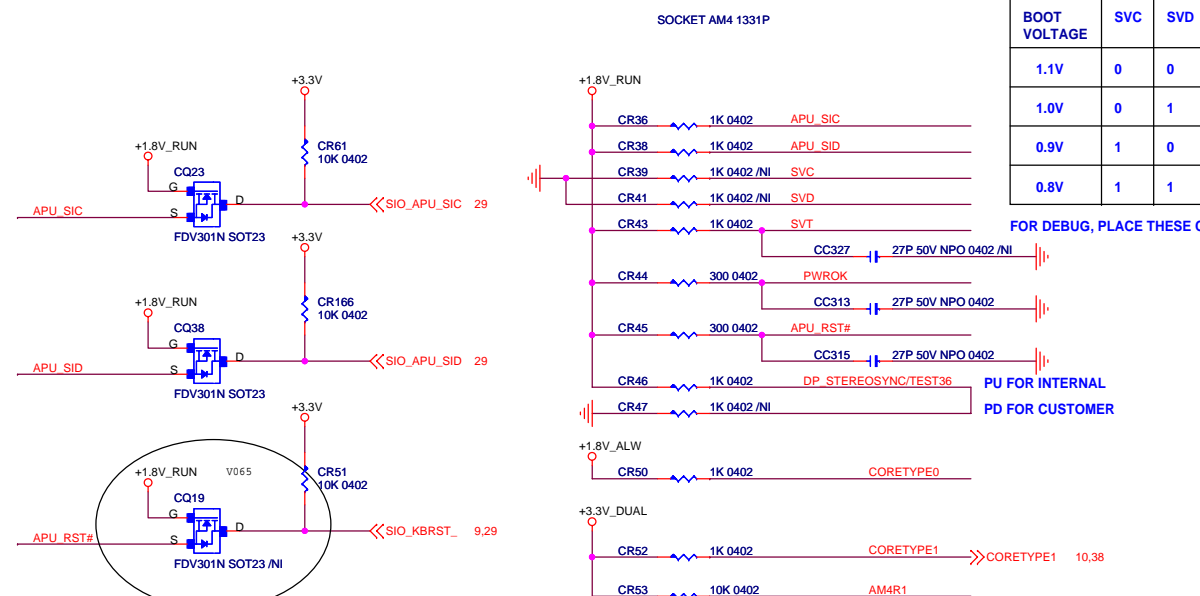
21 DP1_TXP0
21 DP1_TXN0
21 DP1_TXP1
21 DP1_TXN1
21 DP1_TXP2
21 DP1_TXN2
21 DP1_TXP3
21 DP1_TXN3



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CORETYPE DEFINITION	CORETYPE 1	CORETYPE 0	
Family 15h Models 60h-6Fh	0	0	Type0 : 1.8V
Family 17h Models 00h-0Fh	1	0	Type2 : 3.3V
Family 17h Models 10h-1Fh	1	1	Type3 : 3.3V

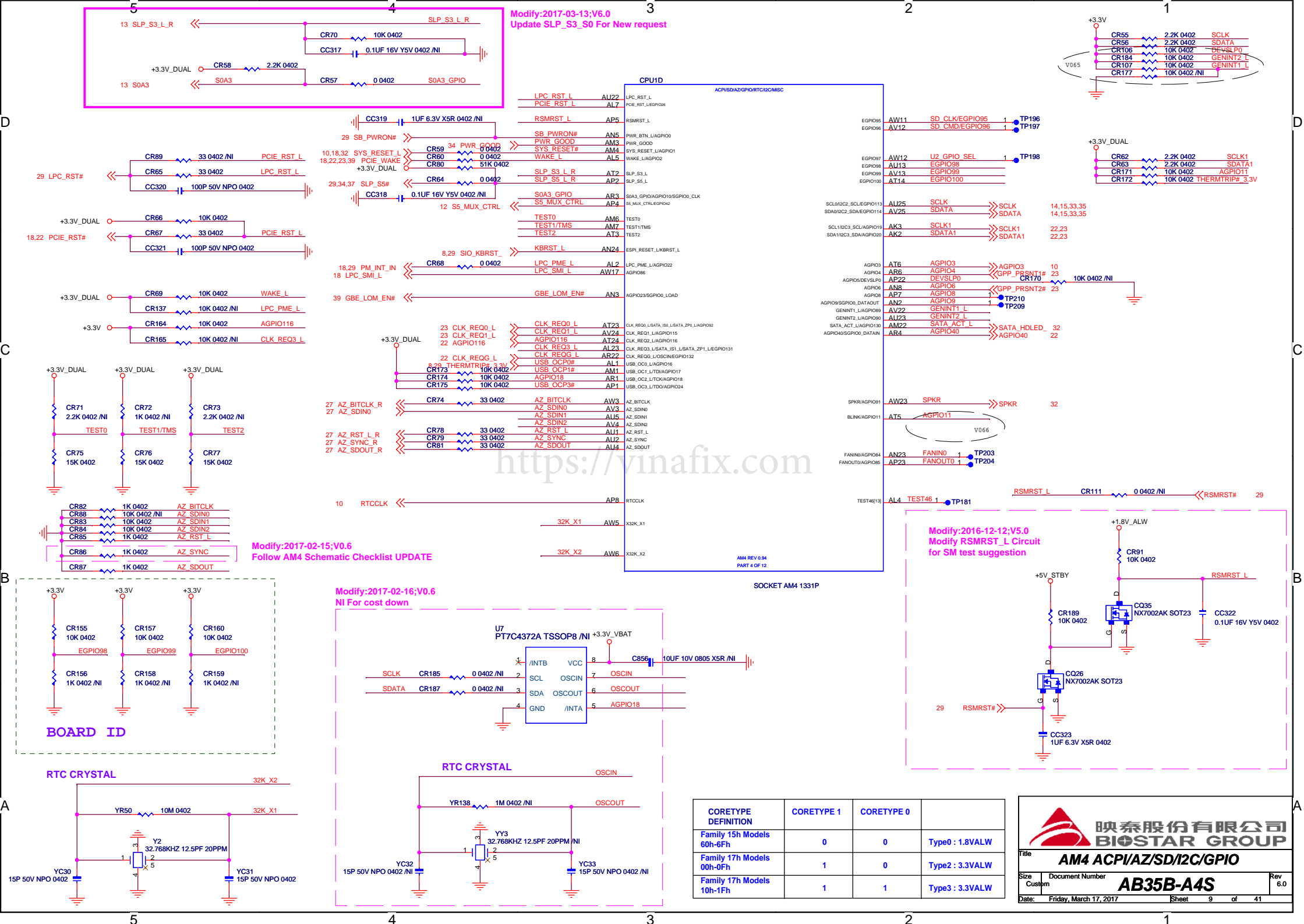


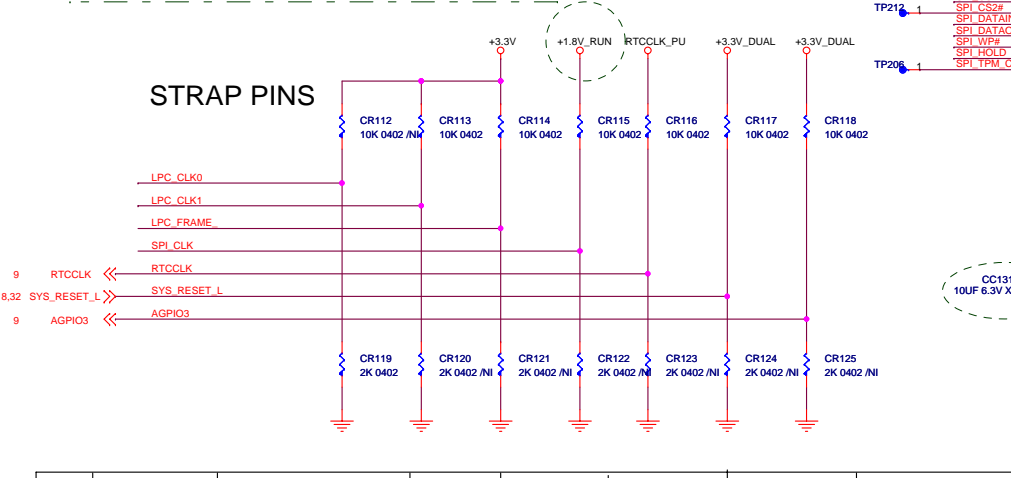
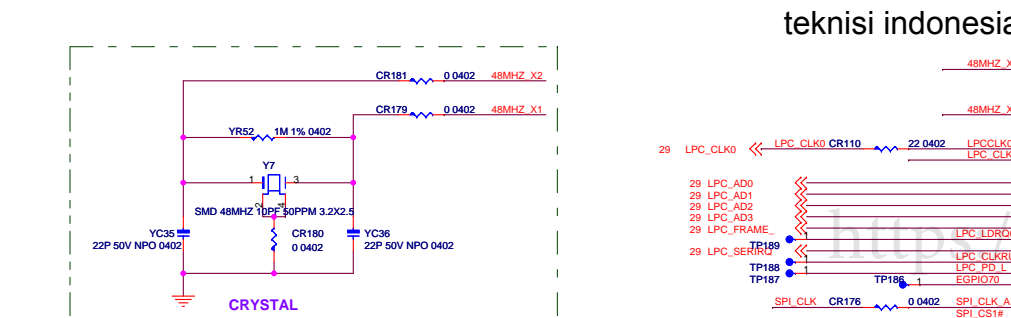
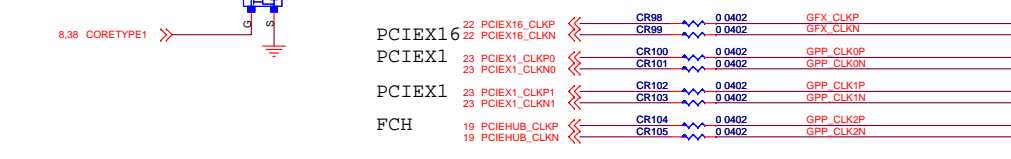
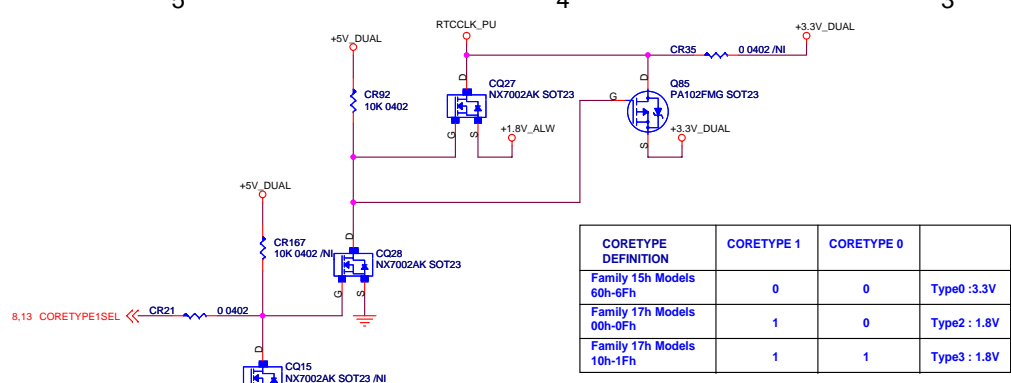
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BIOSAR GROUP

Title **AM4 DISPLAY/MISC**

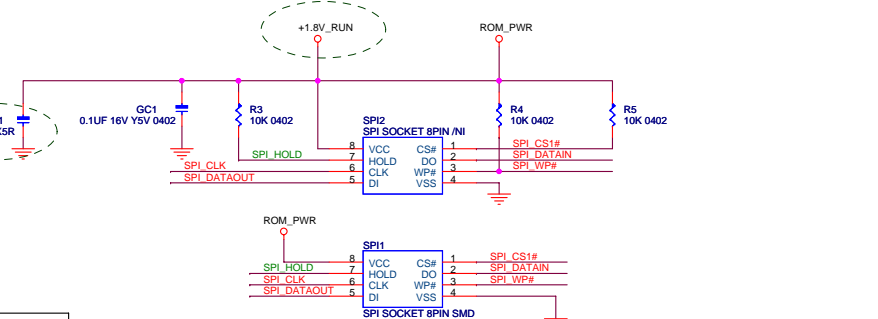
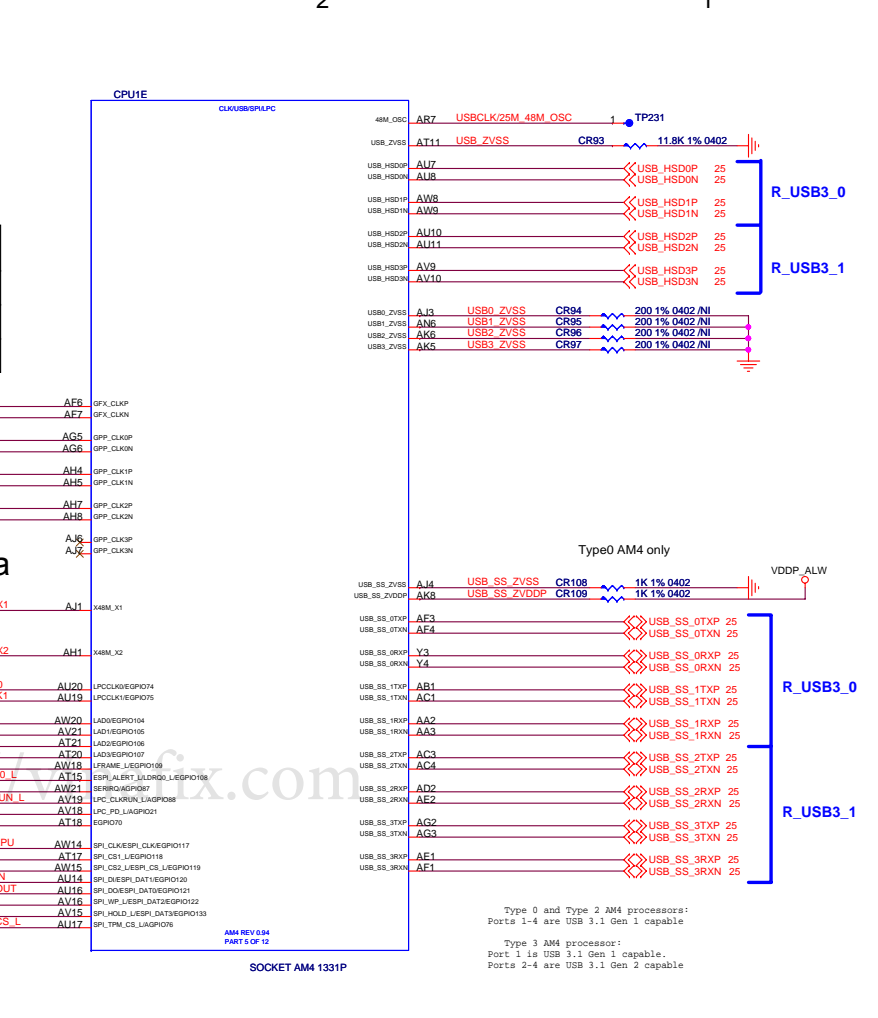
Size Document Number **AB35B-A4S** Rev 6.0

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	LPC_CLK0	LPC_CLK1	AGPIO3	RTC_CLK	LFRAME_L	SYS_RST#	SPI CLK (ZP)
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)	Enhanced reset logic (for quicker S5 S5 resume) (DEFAULT)	Coin battery is on board (DEFAULT)	SPI ROM (DEFAULT)	normal reset mode (DEFAULT)	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLED	Use 100Mhz PCIE clock as reference clock and generate internal clocks only (DEFAULT)	Default to traditional reset logic	Coin battery is not on board.	LPC ROM	short reset mode	Use 100Mhz PCIE clock as reference clock and generate internal clocks only



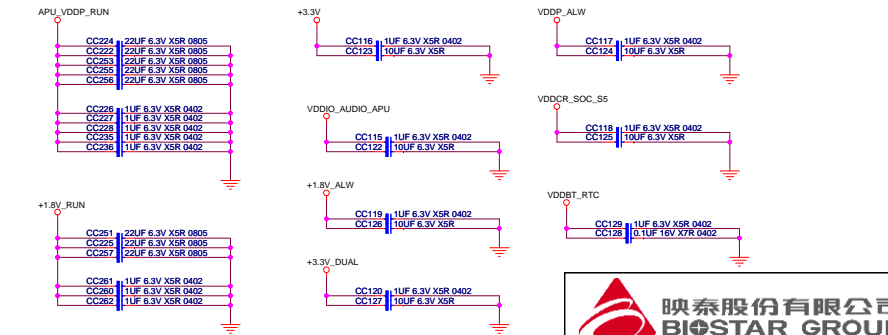
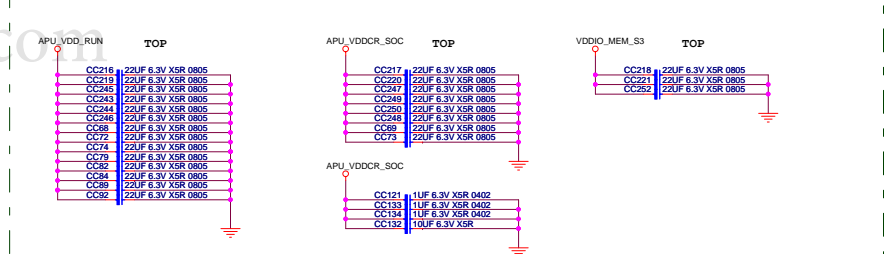
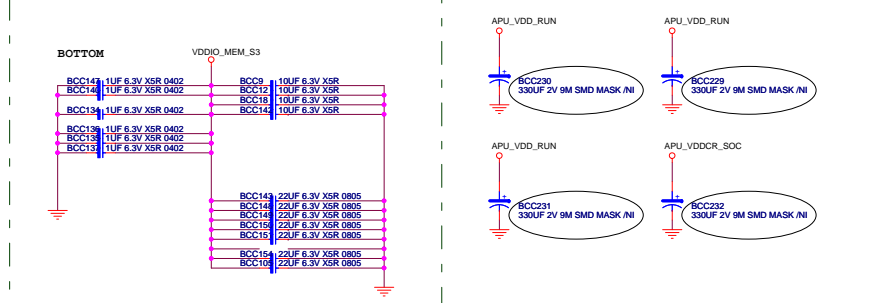
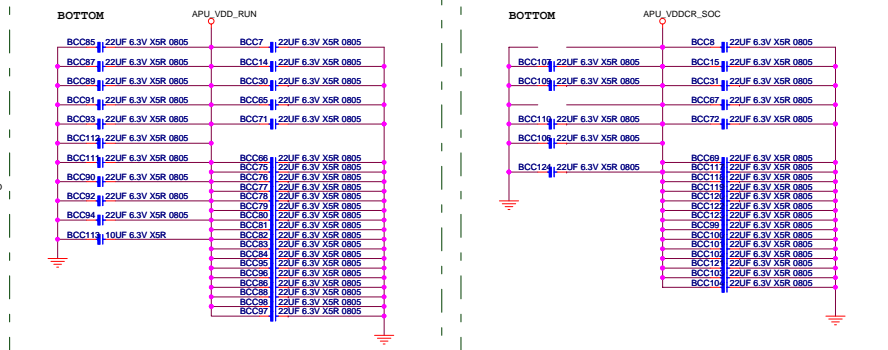
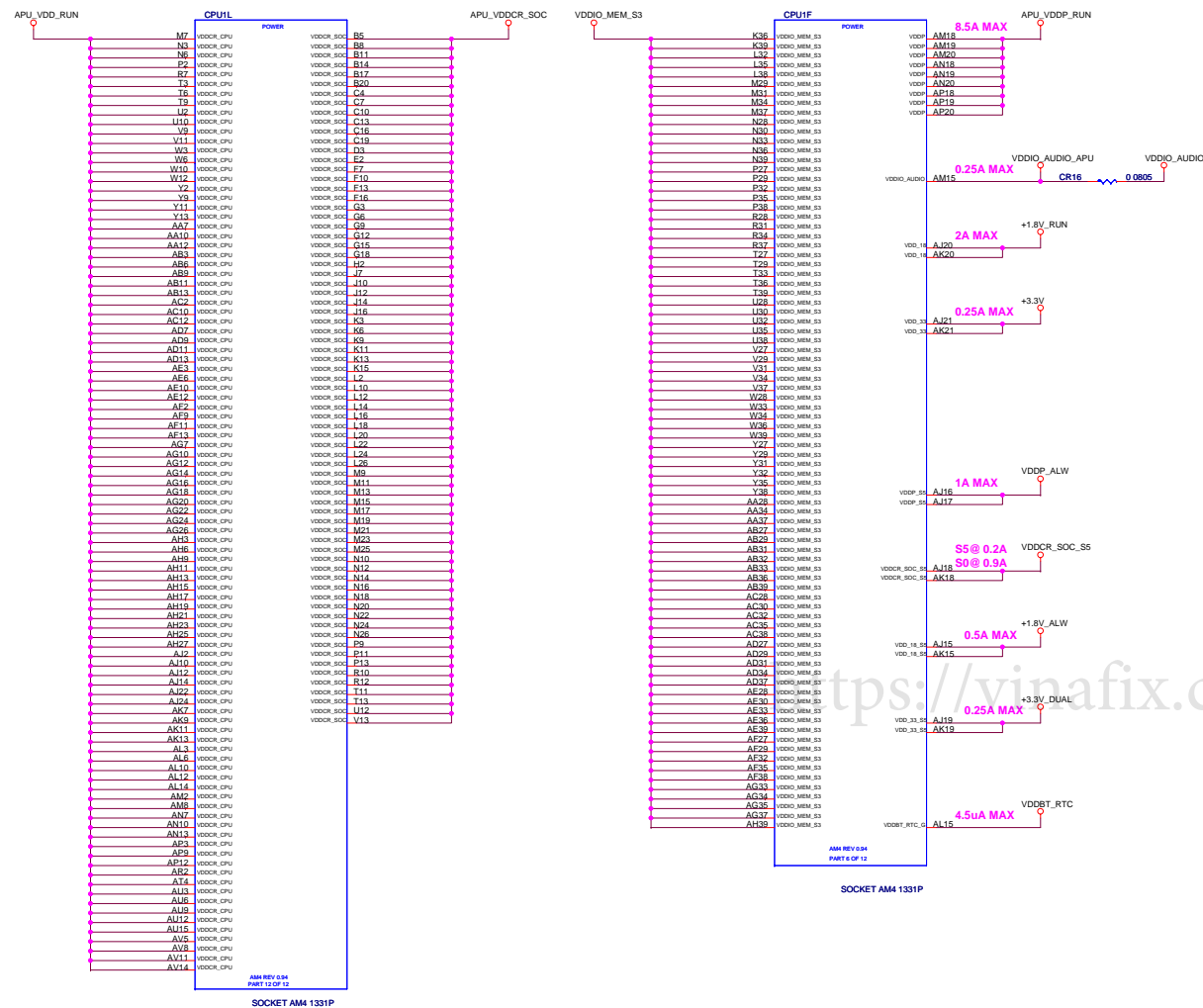
	LPC_CLK0	LPC_CLK1	AGPIO3	RTC_CLK	LFRAME_L	SYS_RST#	SPI CLK (ZP)
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)	Enhanced reset logic (for quicker S5 S5 resume) (DEFAULT)	Coin battery is on board (DEFAULT)	SPI ROM (DEFAULT)	normal reset mode (DEFAULT)	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLED	Use 100Mhz PCIE clock as reference clock and generate internal clocks only (DEFAULT)	Default to traditional reset logic	Coin battery is not on board.	LPC ROM	short reset mode	Use 100Mhz PCIE clock as reference clock and generate internal clocks only

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Title: AM4 CLK/LPC/SPI/USB

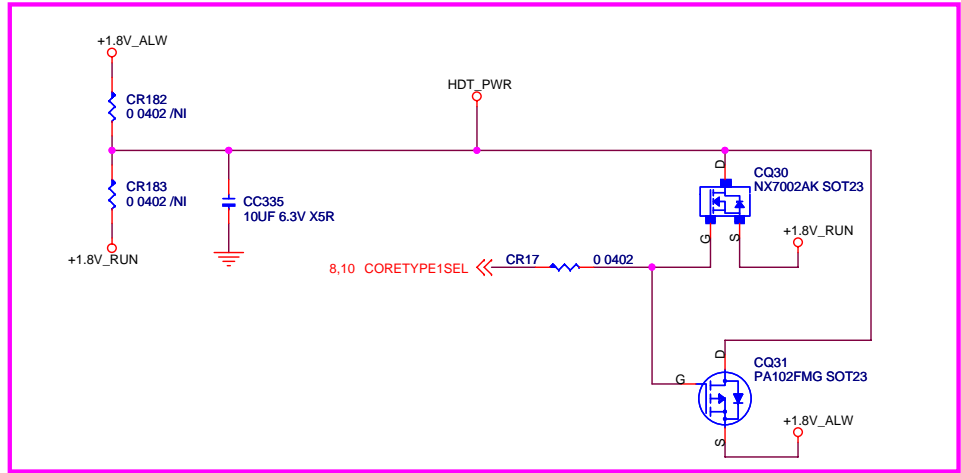
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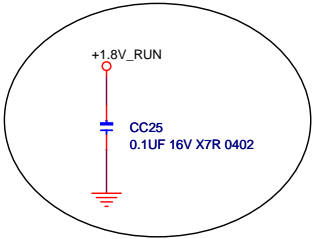




Modify:2017-03-08;V6.0
Follow DEMO For Summit CPU +1.8V_RUN Leakage issue

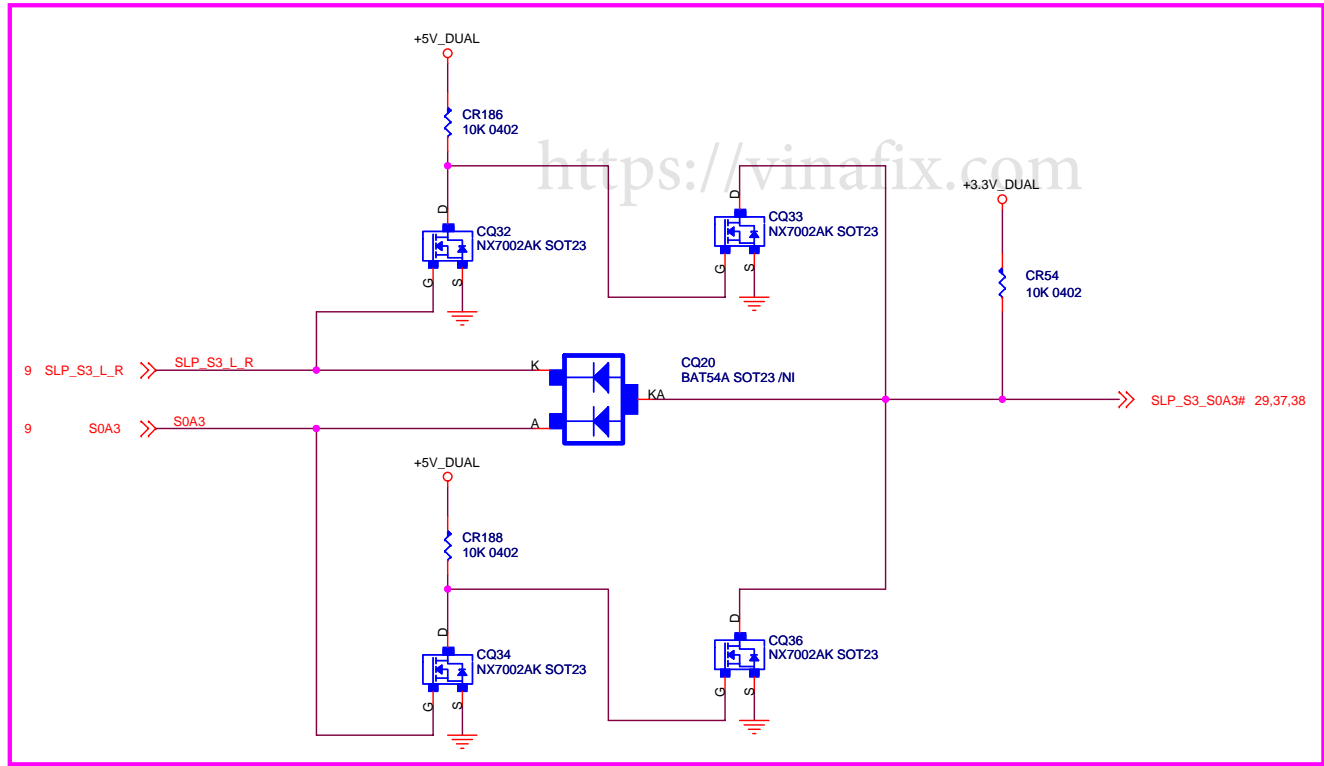


CORETYPE DEFINITION	CORETYPE 1	CORETYPE 0	
Family 15h Models 60h-6Fh	0	0	Type0 : 1.8V
Family 17h Models 00h-0Fh	1	0	Type2 : 1.8VALW
Family 17h Models 10h-1Fh	1	1	Type3 : 1.8VALW



Place close to CR183

Modify:2017-03-13;V6.0
Update SLP_S3_S0 For New request

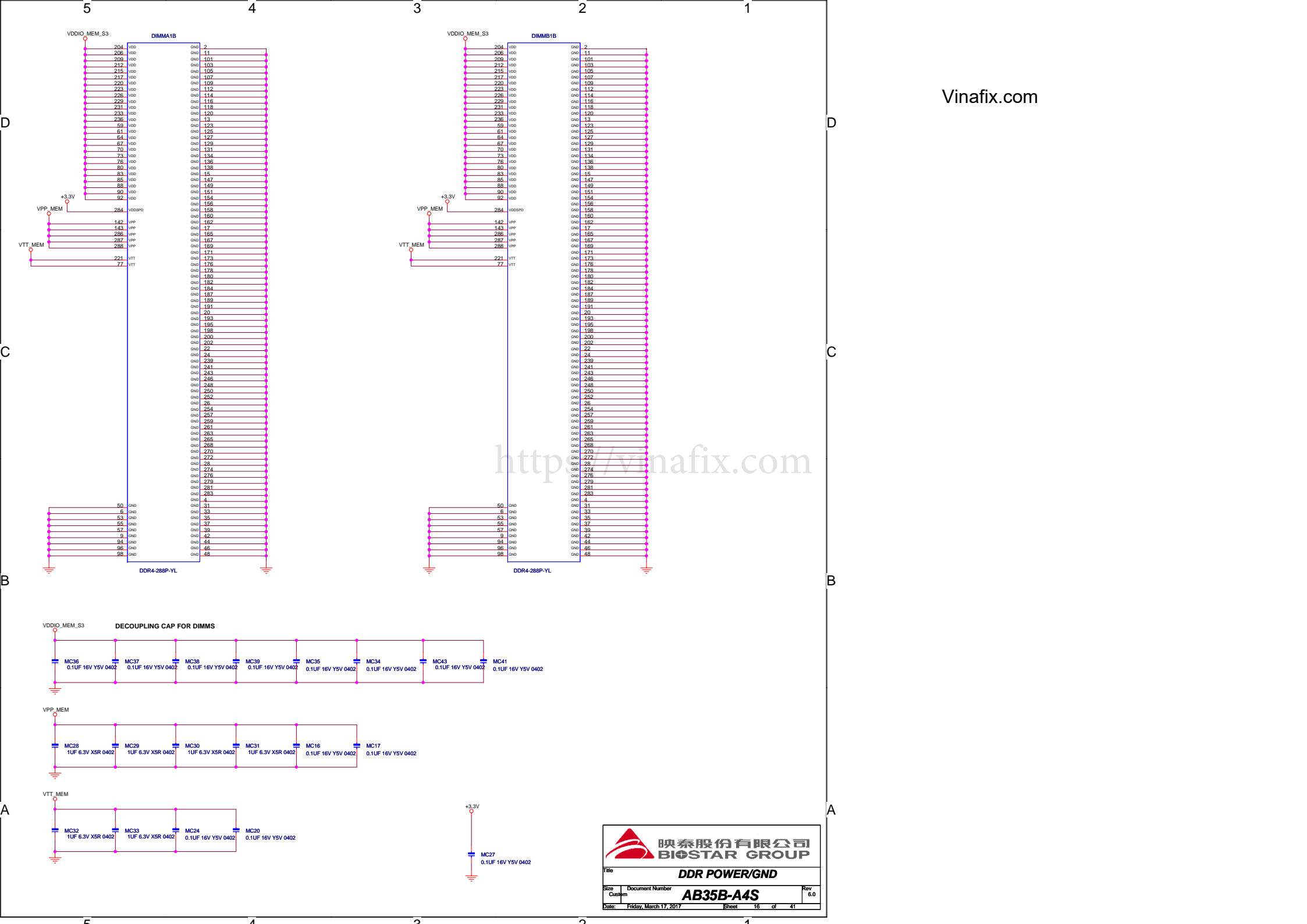


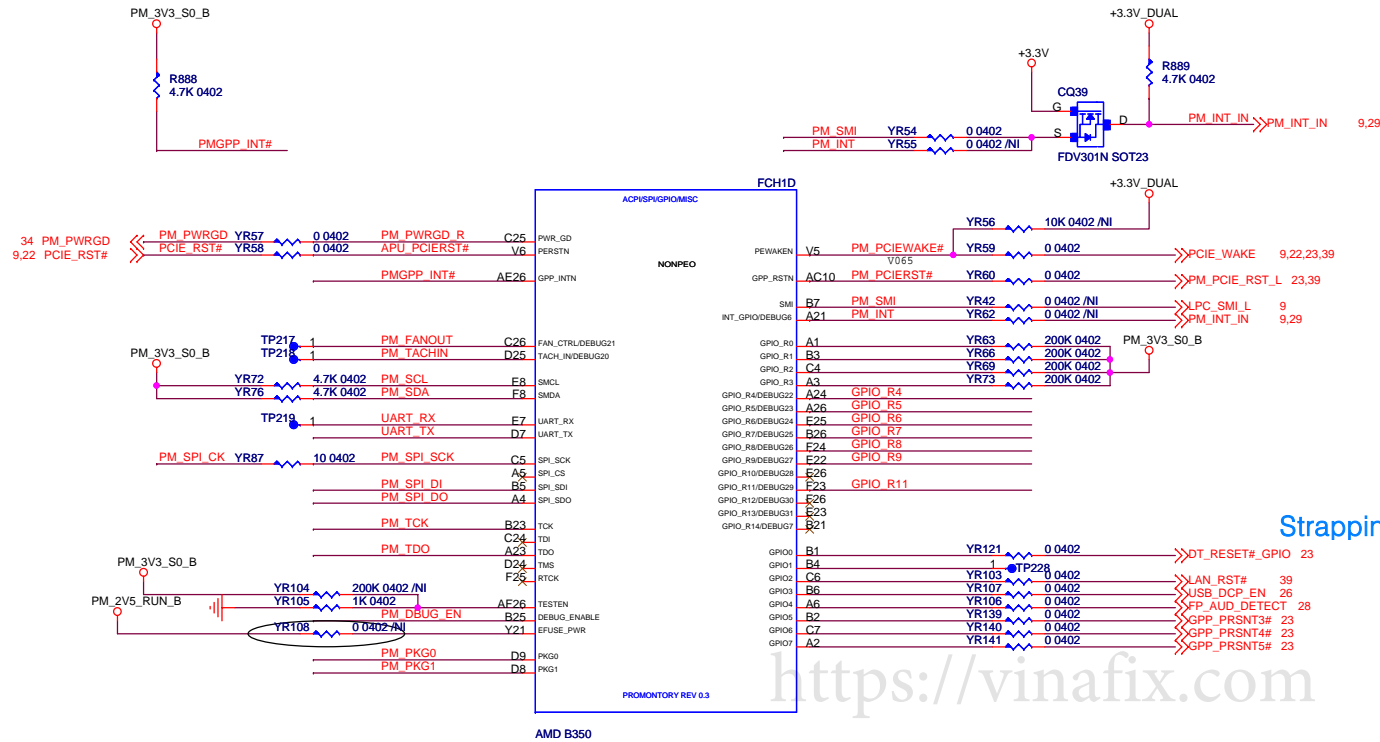
Title AM4 DEBUG			
Size B	Document Number AB35B-A4S		Rev 6.0
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SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMA1	A4
DIMMB0	A2
DIMMB1	A6

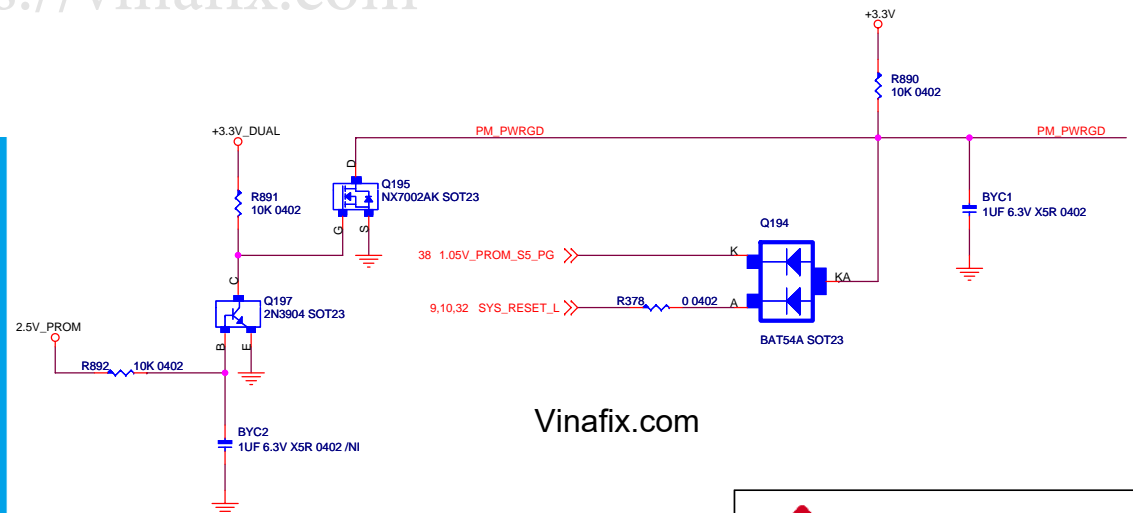
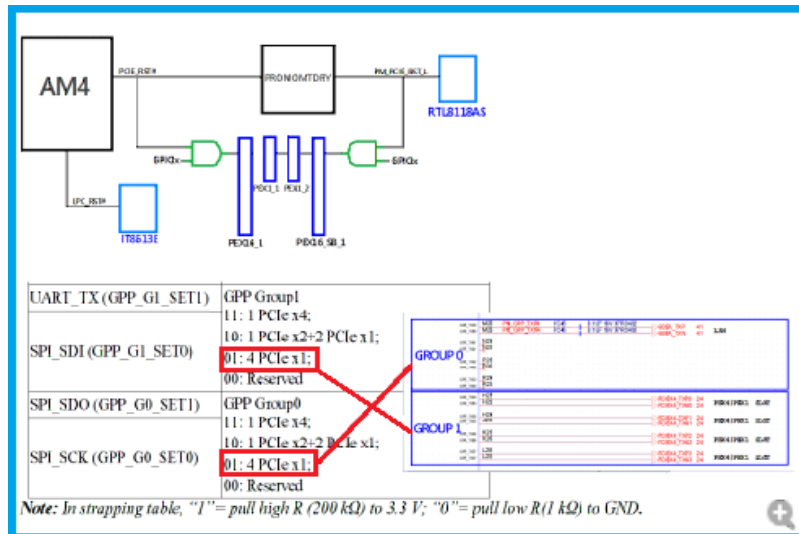
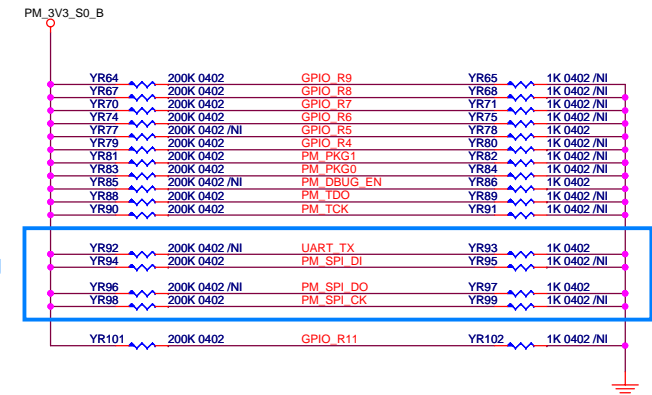






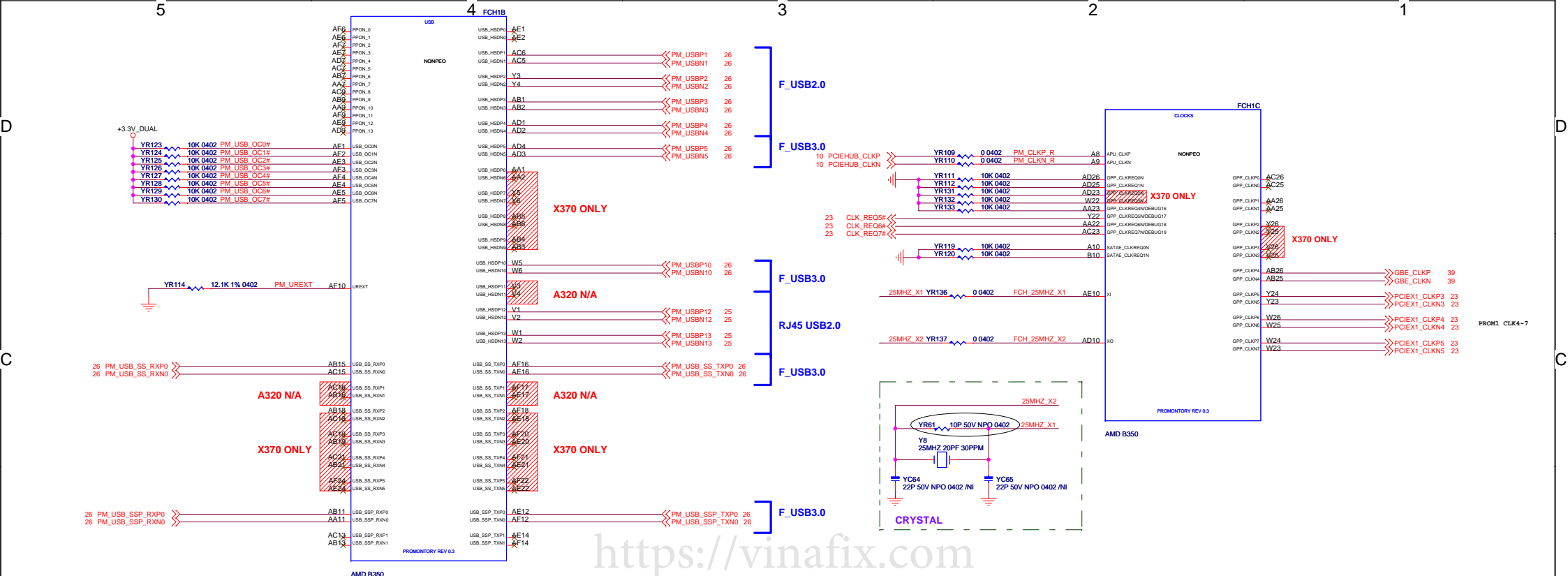
GROUP0	PM_SPI_DO	PM_SPI_CK	LANE0	LANE1	LANE2	LANE3
0	1		X1	X1	X1	X1
1	0		X2		X1	X1
1	1		X4			

GROUP1	UART_TX	PM_SPI_DI	LANE4	LANE5	LANE6	LANE7
0	1		X1	X1	X1	X1
1	0		X2		X1	X1
1	1		X4			



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Title: FCH-PCIE/PCI/APU/LPC/CK			
Size: Custom	Document Number: AB35B-A4S	Rev: 6.0	
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USB Port to OC Pin Mapping	
USB3.1	USB2.0
USB_SSP_TXRX[0]	USB_HSD[5]
USB_SSP_TXRX[1]	USB_HSD[0]
USB3.0	USB2.0
USB_SS_TXRX[0]	USB_HSD[10]
USB_SS_TXRX[1]	USB_HSD[11]
USB_SS_TXRX[2]	USB_HSD[6]
USB_SS_TXRX[3]	USB_HSD[7]
USB_SS_TXRX[4]	USB_HSD[8]
USB_SS_TXRX[5]	USB_HSD[9]
	USB_HSD[1]
	USB_HSD[2]
	USB_HSD[3]
	USB_HSD[4]
	USB_HSD[12]
	USB_HSD[13]

USB	
BUS Model	USB
	3.1 Gen2 10 Gbps
	3.1 Gen1 5 Gbps
	2.0
	Debug Port
PROM4	USB_SSP Port0~1
PROM2	USB_SSP Port0~1
PROM1	USB_SSP Port0

SATA	
BUS Model	SATA
	SATA 3.0
	SATA Express
	PCI Express® Gen2 GPP
	PCI Express® CLK
PROM4	SATA port0~3
PROM2	SATA port0~1
PROM1	SATA port0~1

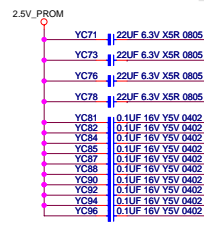
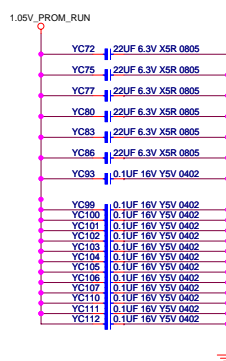
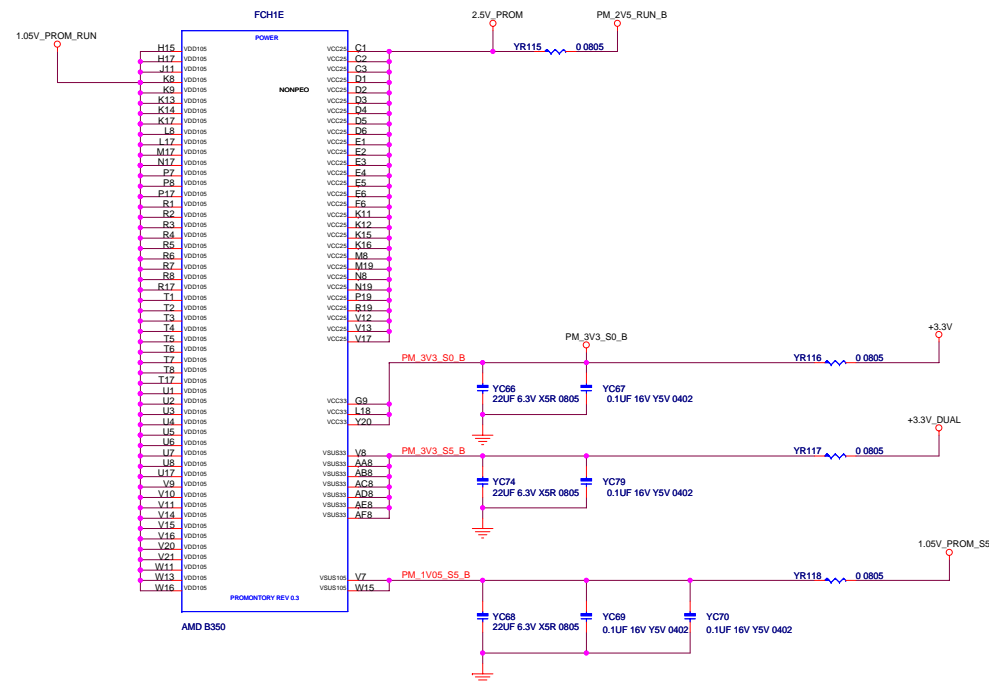
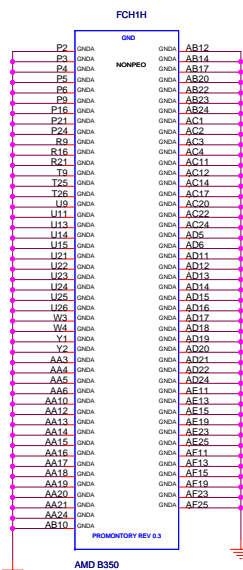
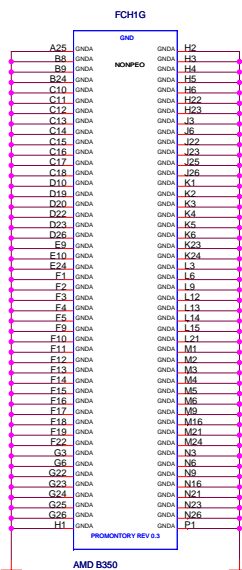
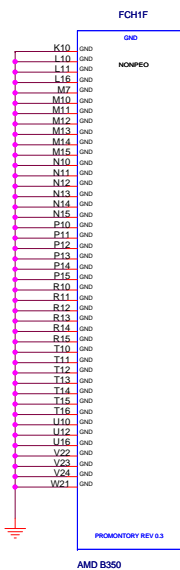
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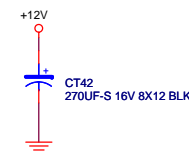
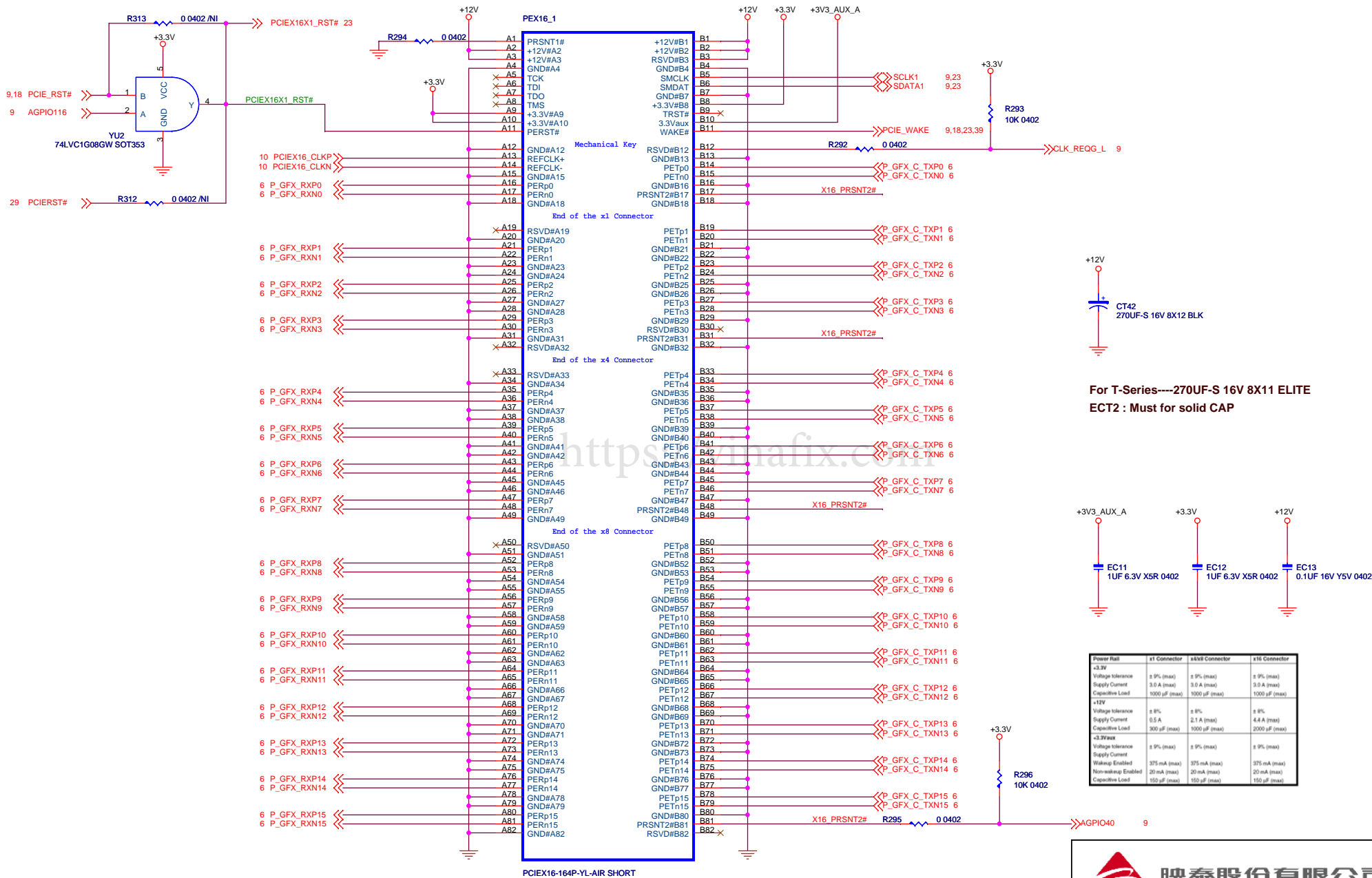
Date: Friday, March 17, 2017

Rev: 6.0

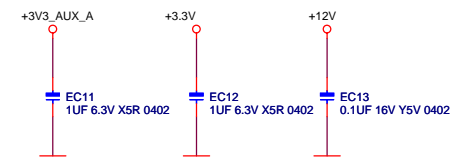


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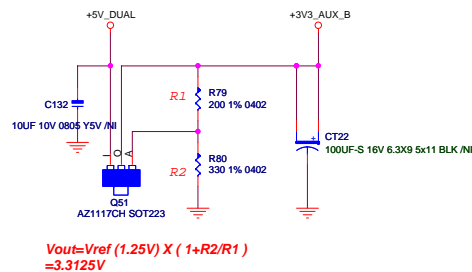
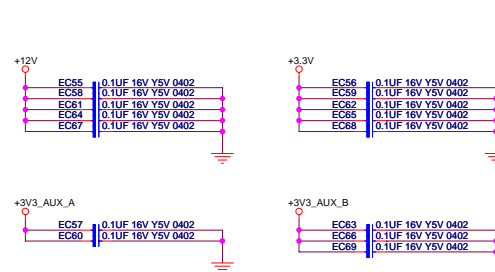
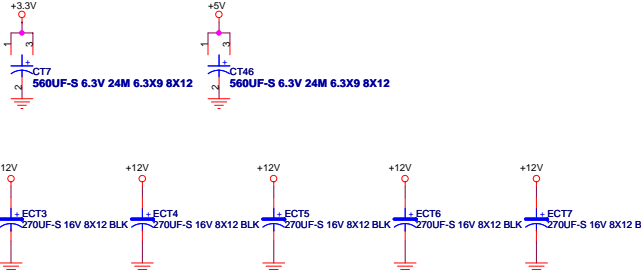
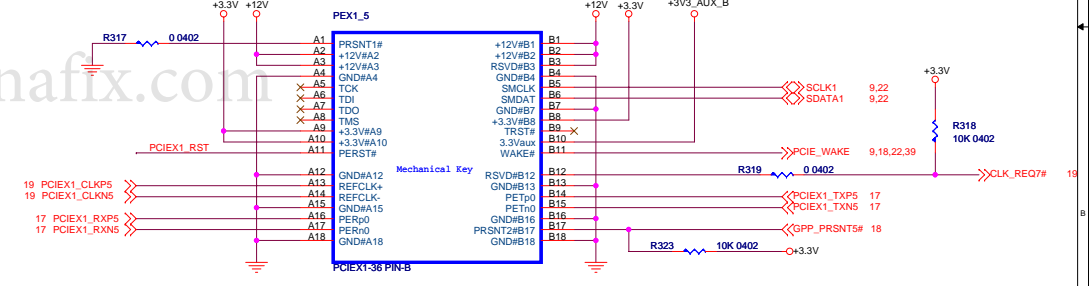
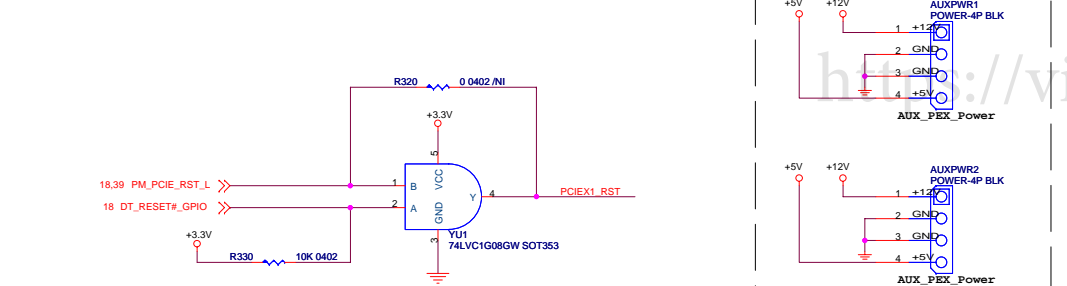
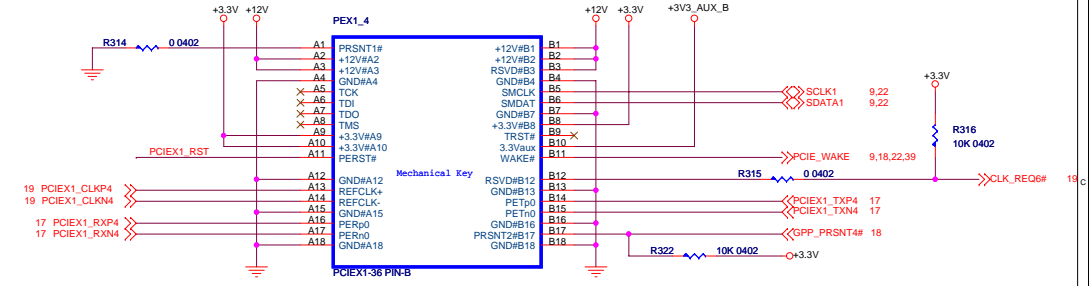
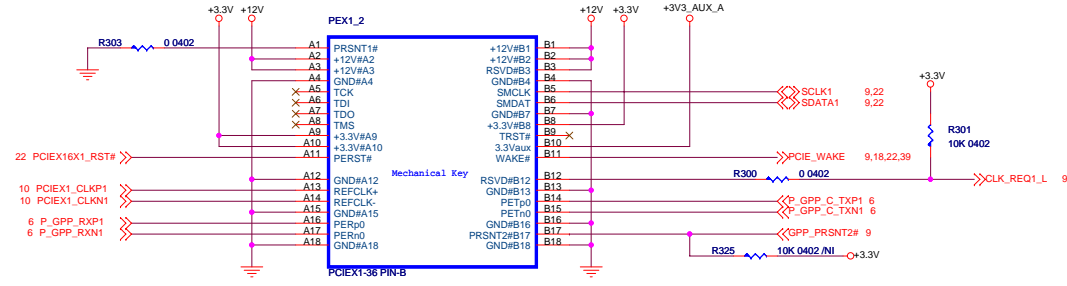
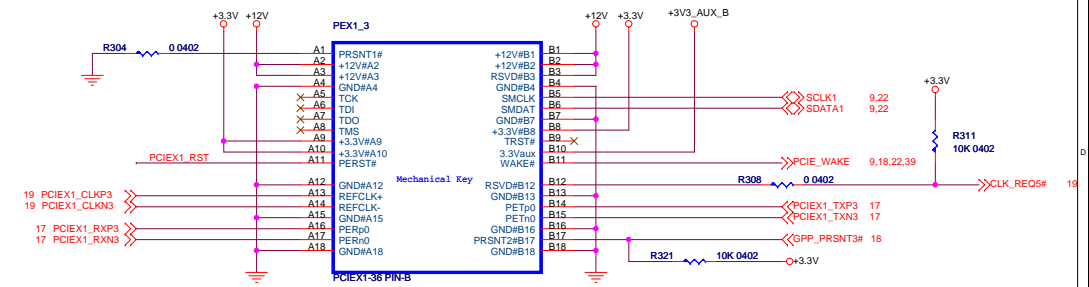
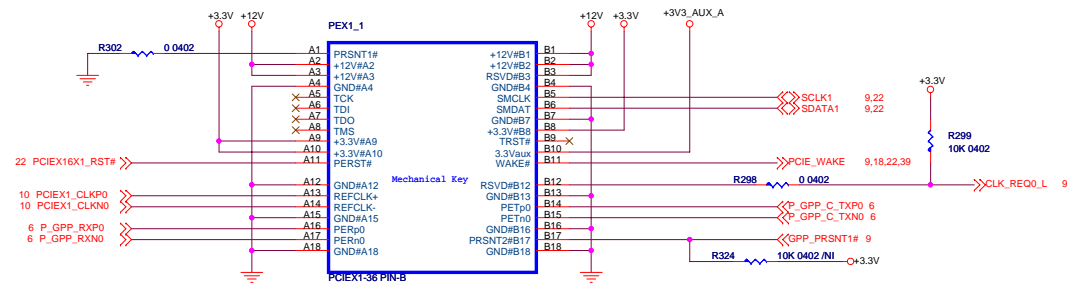


For T-Series----270UF-S 16V 8X11 ELITE
ECT2 : Must for solid CAP



Power Rail	x1 Connector	x8/x16 Connector	x16 Connector
+3.3V			
Voltage tolerance	± 9% (max)	± 9% (max)	± 9% (max)
Supply Current	3.0 A (max)	3.0 A (max)	3.0 A (max)
Capacitive Load	1000 µF (max)	1000 µF (max)	1000 µF (max)
+12V			
Voltage tolerance	± 8%	± 8%	± 8%
Supply Current	0.5 A	2.1 A (max)	4.4 A (max)
Capacitive Load	300 µF (max)	1000 µF (max)	2000 µF (max)
+3.3Vaux			
Voltage tolerance	± 9% (max)	± 9% (max)	± 9% (max)
Supply Current	375 mA (max)	375 mA (max)	375 mA (max)
Wakeup Enabled	20 mA (max)	20 mA (max)	20 mA (max)
Non-wakeup Enabled	150 µF (max)	150 µF (max)	150 µF (max)

Title PEX16 SLOT		
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$$V_{out} = V_{ref} (1.25V) \times (1 + R2/R1) = 3.3125V$$

Power Pin	x1 Connector	x18 Connector	x16 Connector
+3.3V			
Voltage Inference	± 9% (max)	± 9% (max)	± 9% (max)
Supply Current	3.0 A (max)	3.0 A (max)	3.0 A (max)
Capacitive Load	1000 µF (max)	1000 µF (max)	1000 µF (max)
+12V			
Voltage Inference	± 9%	± 9%	± 9%
Supply Current	10.0 A	8.1 A (max)	4.4 A (max)
Capacitive Load	300 µF (max)	1000 µF (max)	2000 µF (max)
+3V3_AUX			
Voltage Inference	± 9% (max)	± 9% (max)	± 9% (max)
Supply Current	375 mA (max)	375 mA (max)	375 mA (max)
Wakeup Enabled	30 mA (max)	30 mA (max)	30 mA (max)
Non-wakeup Enabled	150 µF (max)	150 µF (max)	150 µF (max)

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PCIEX1 SLOT

AB35B-A4S

Rev 6.0

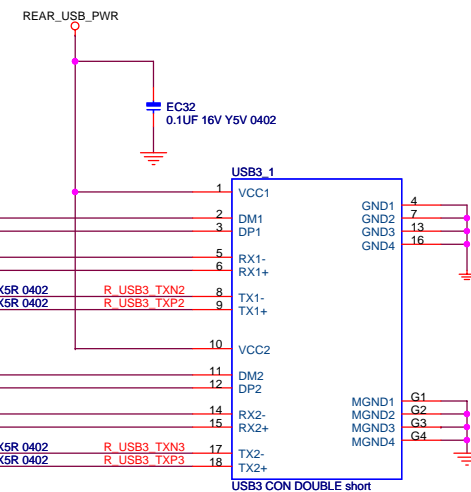
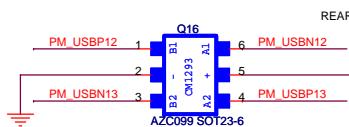
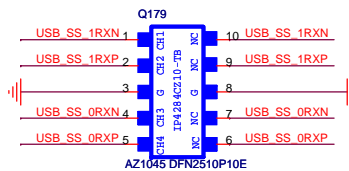
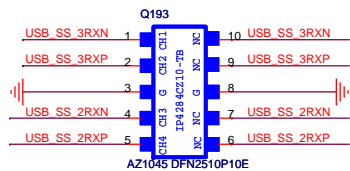
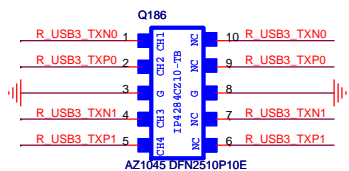
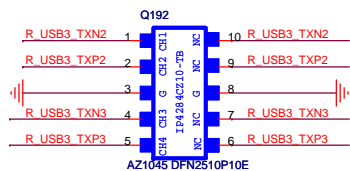
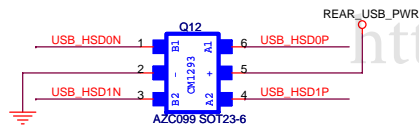
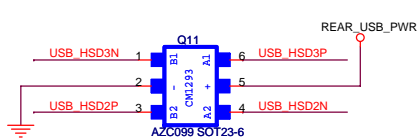
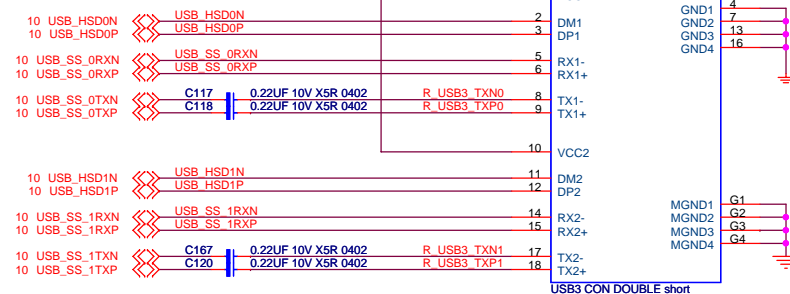
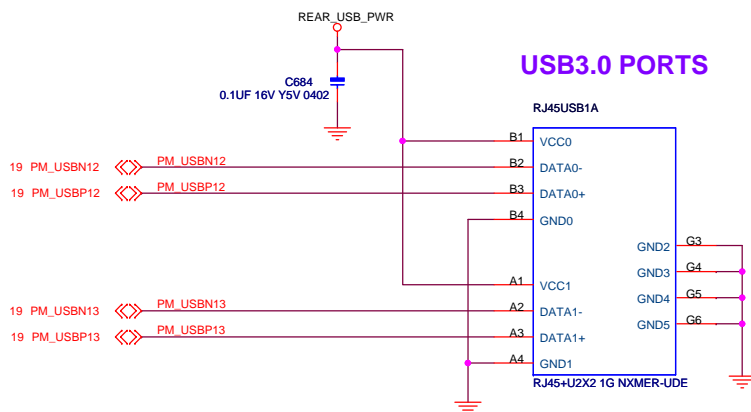
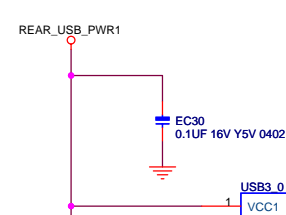
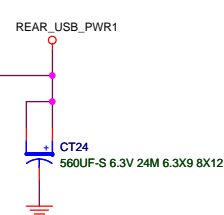
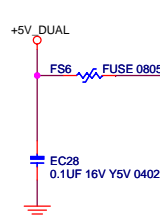
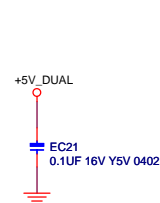
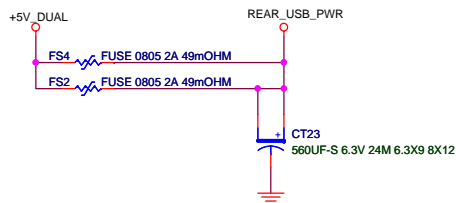
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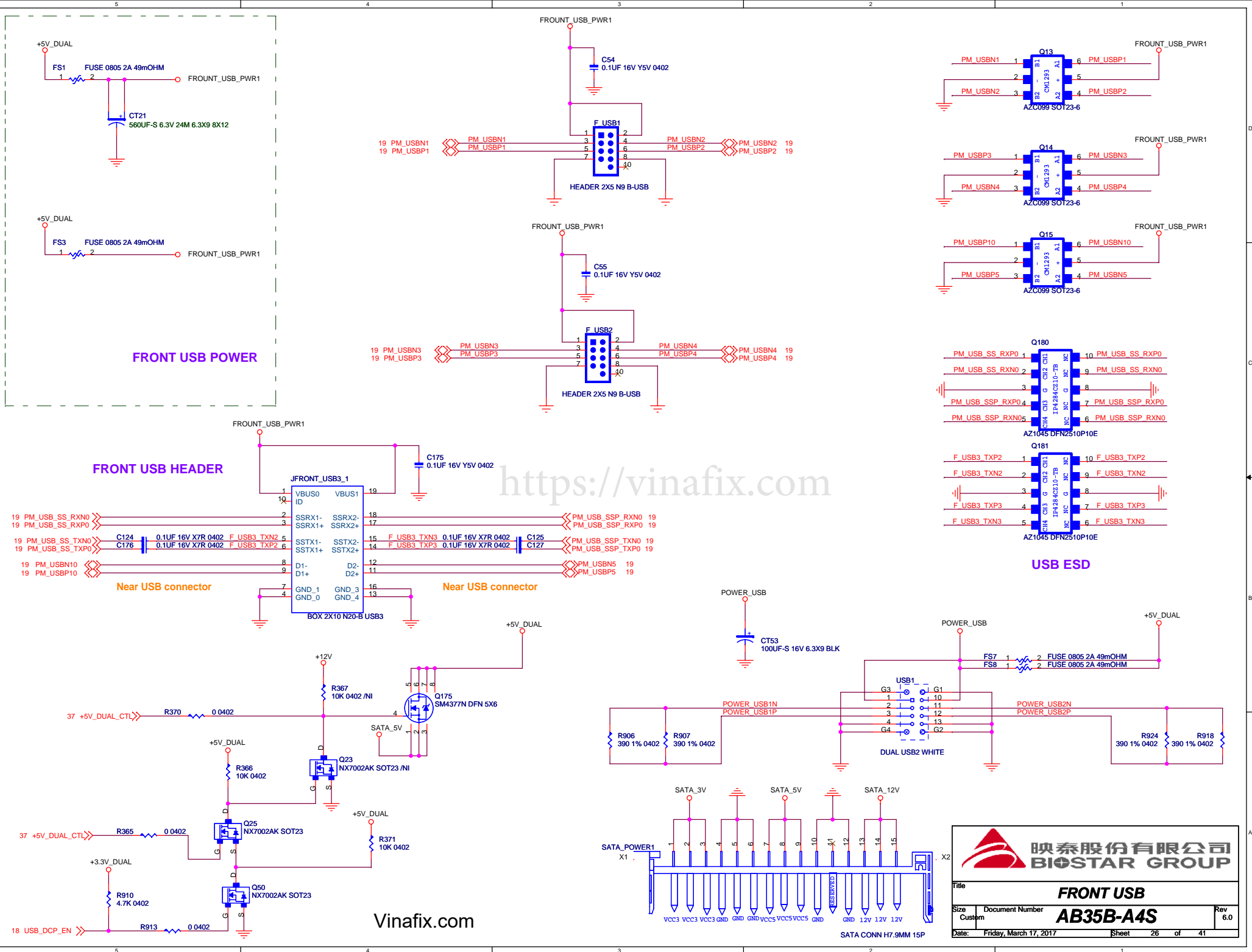
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BIOSTAR GROUP

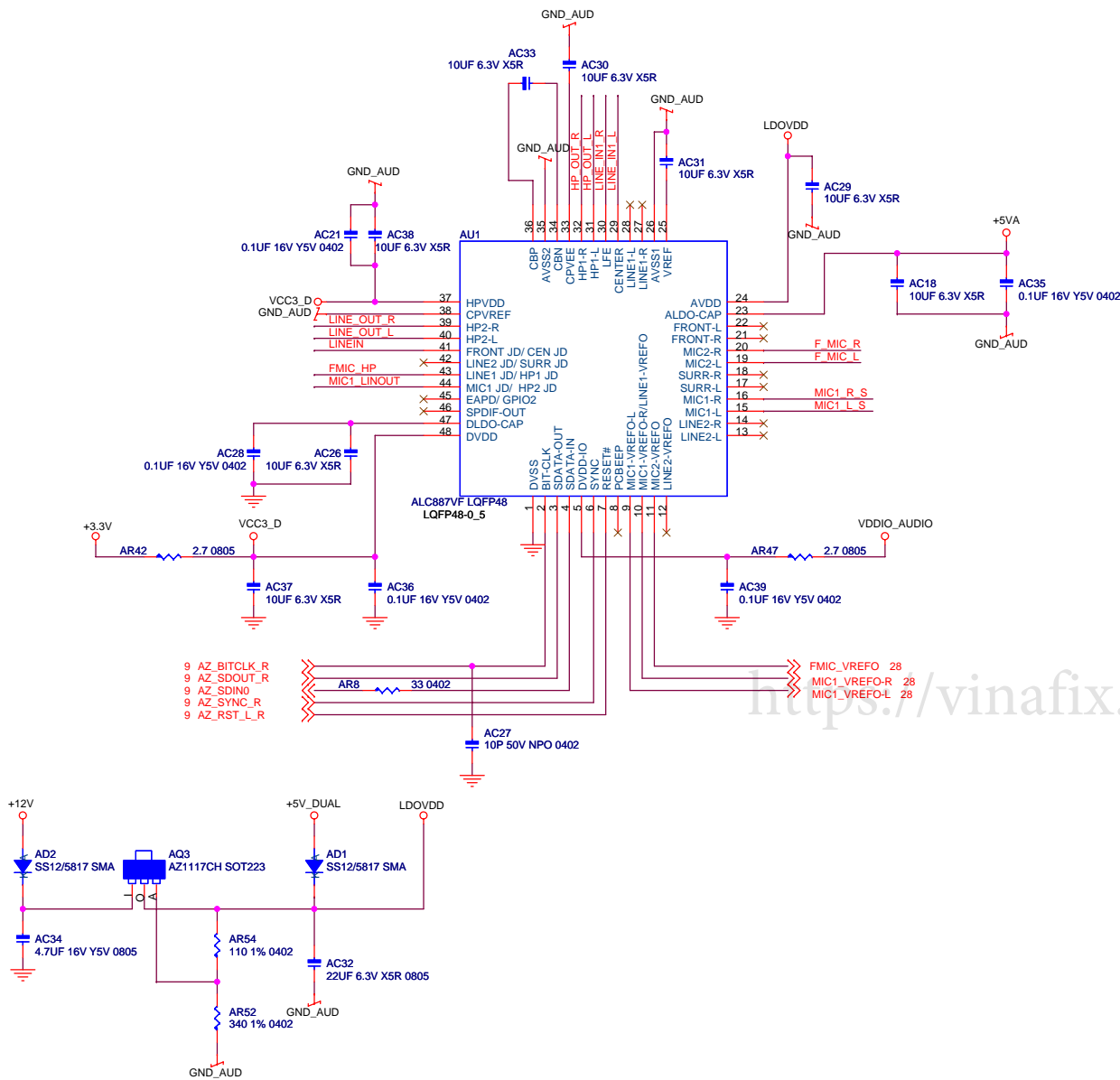
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Size	Document Number				Rev
C	AB35B-A4S				6.0
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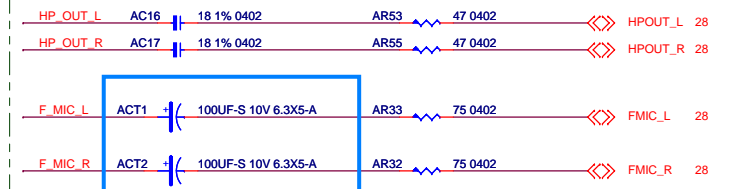
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USB CONN	
Size	Document Number
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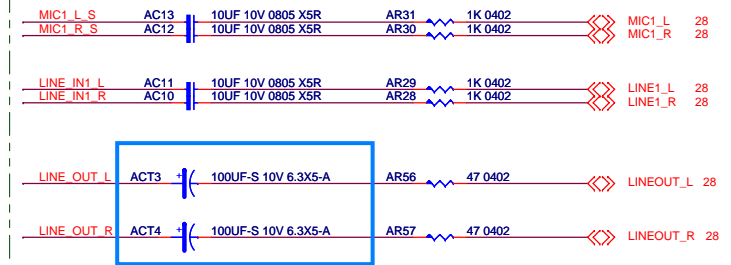


FRONT CHANNEL



Golden EC

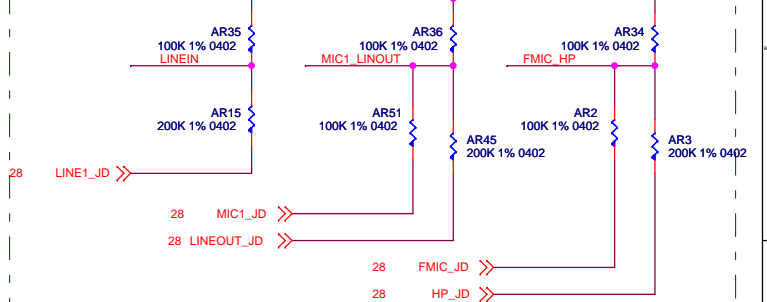
REAR CHANNEL



Golden EC

JD Group

as close as possible to AU1



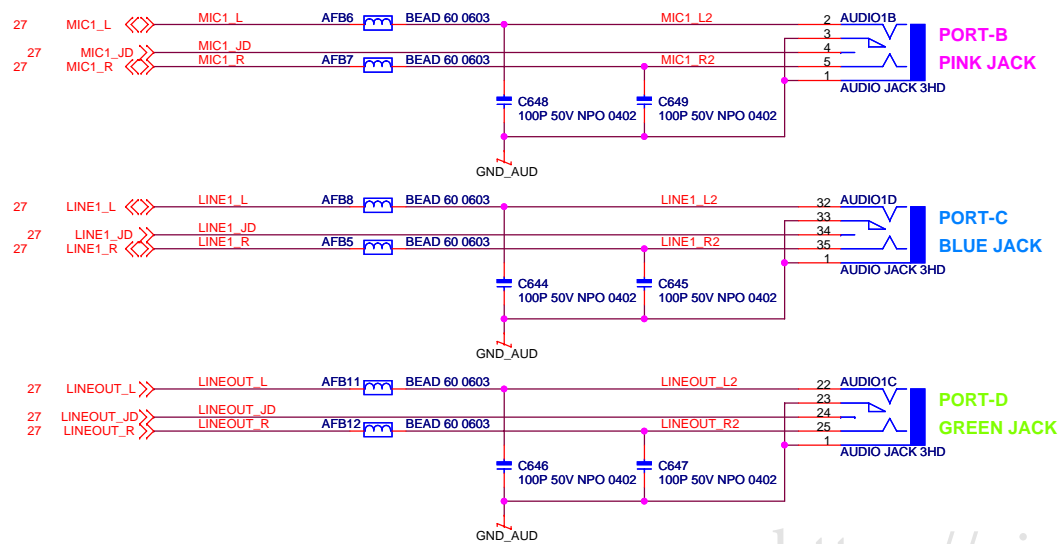
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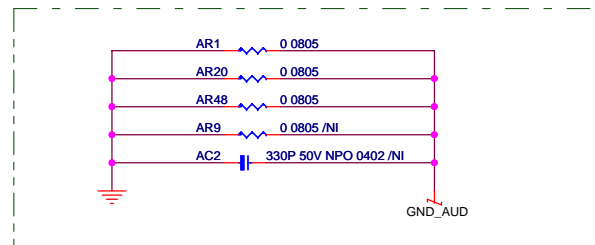


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Size	Document Number	Rev	
Custom	AB35B-A4S	6.0	
Date:	Friday, March 17, 2017	Sheet	27 of 41

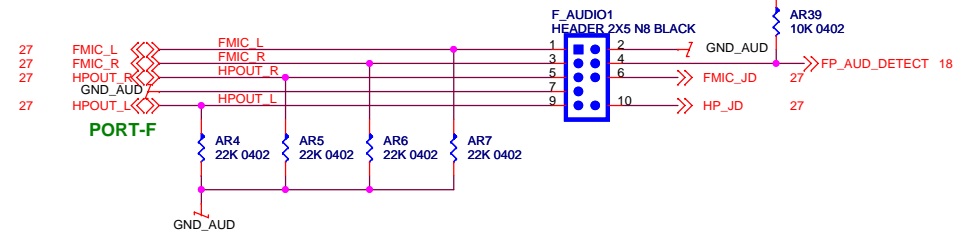
REAR AUDIO JACKS



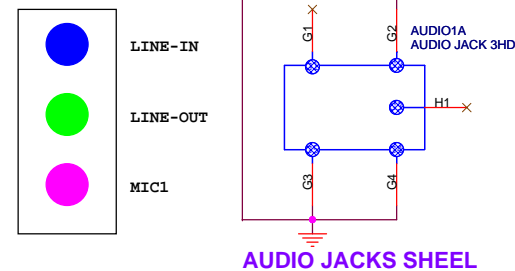
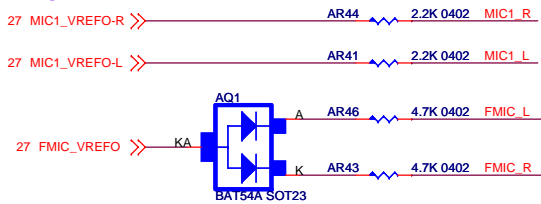
EMI Solution



FRONT AUDIO HEADER



MIC VREF

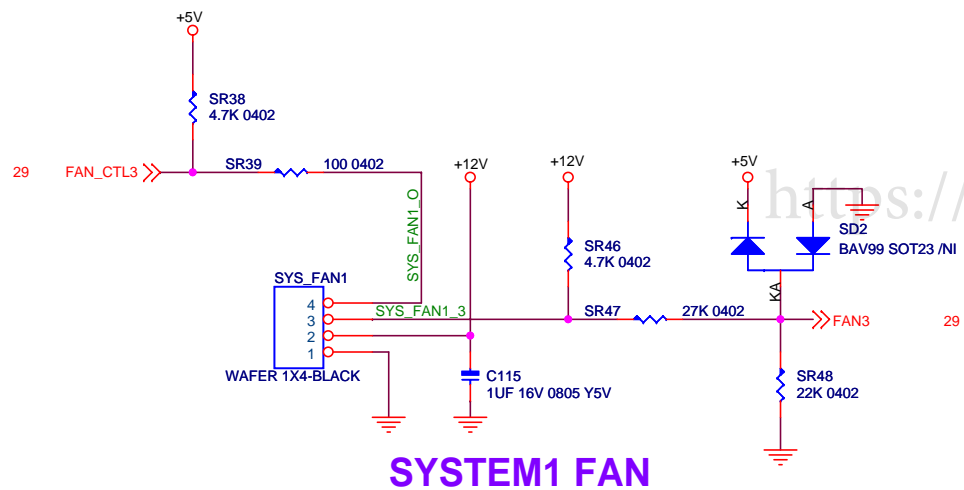
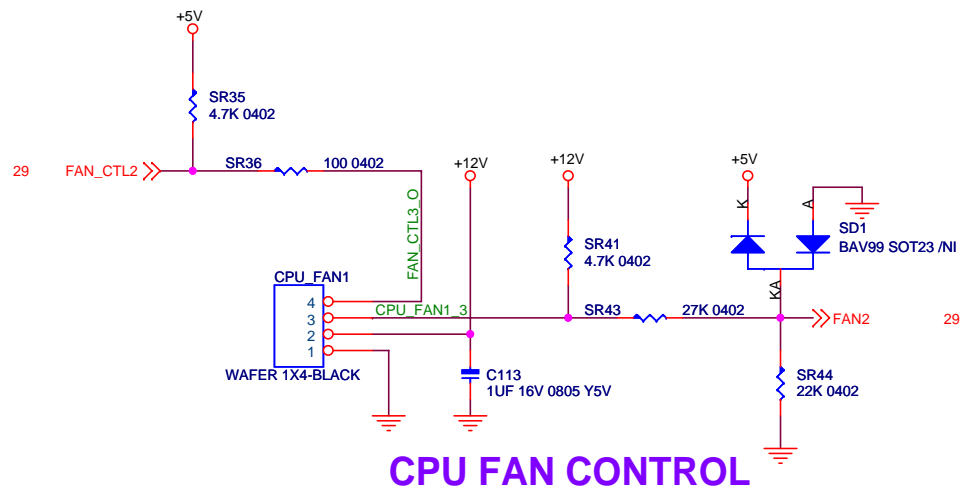



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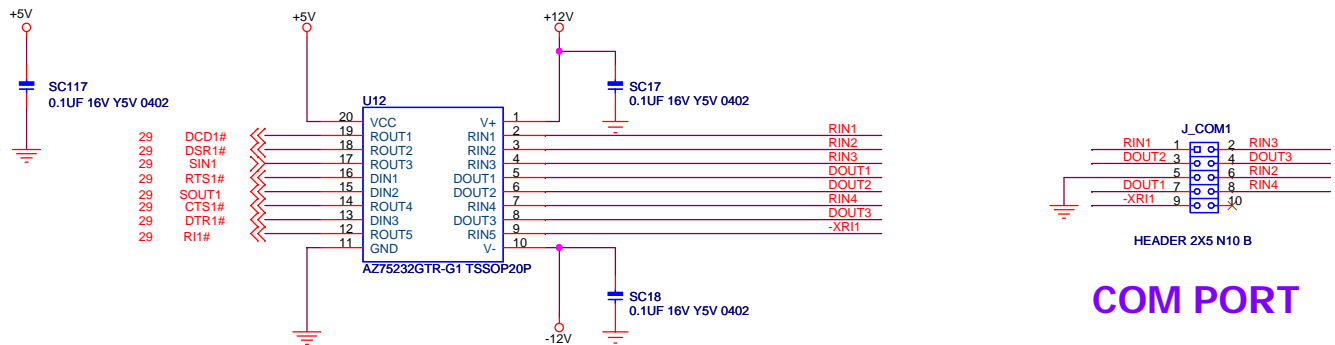
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Size Custom	Document Number AB35B-A4S	Rev 6.0
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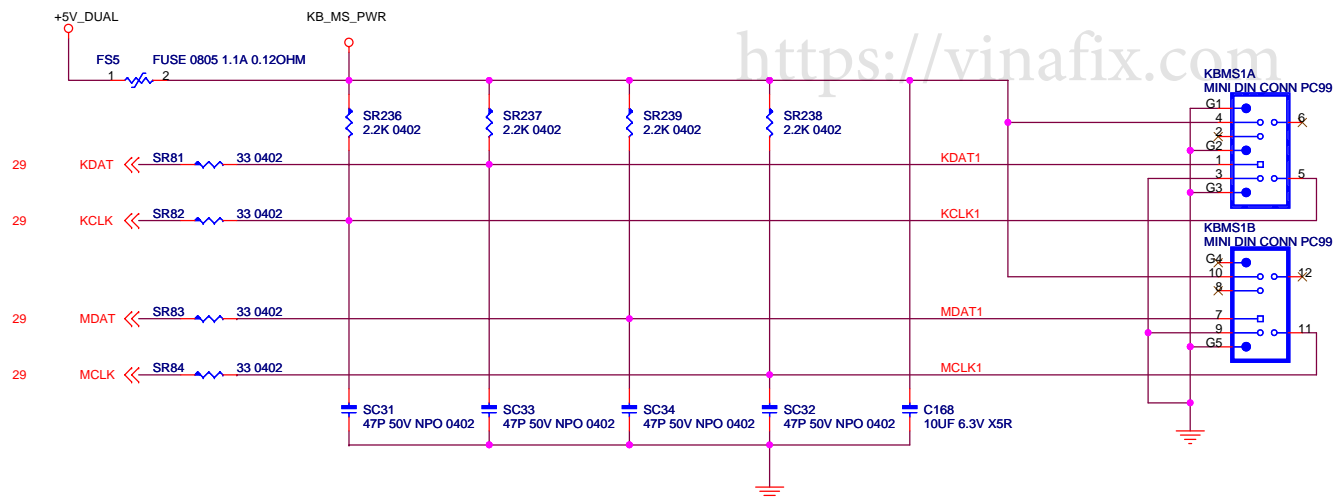


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Size Custom	Document Number AB35B-A4S		Rev 6.0
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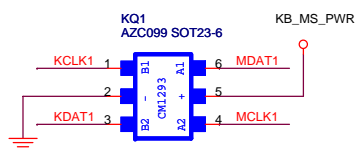


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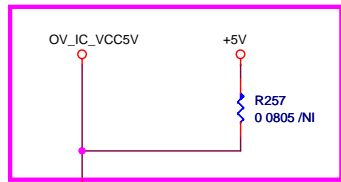
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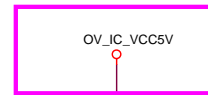
KEYBOARD & MOUSE



 映泰股份有限公司 BIOSSTAR GROUP			
Title			
COM Header/PS2			
Size	Document Number	Rev	
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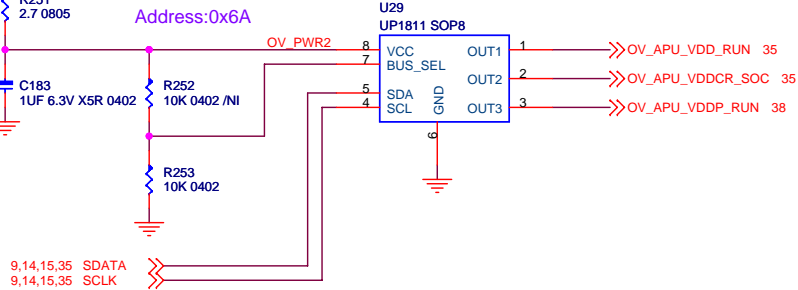


Modify:2017-03-13;V6.0
Add OV_IC_VCC5V circuit To keep VCC for OV IC during S3

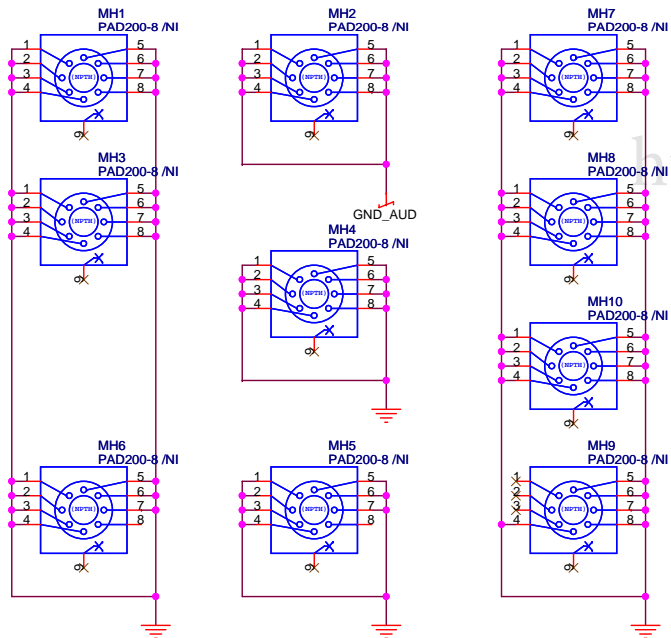


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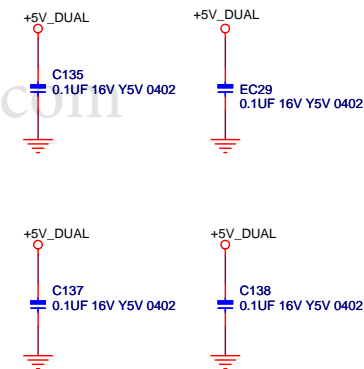
U30
UP1811 SOP8



Vinafix.com



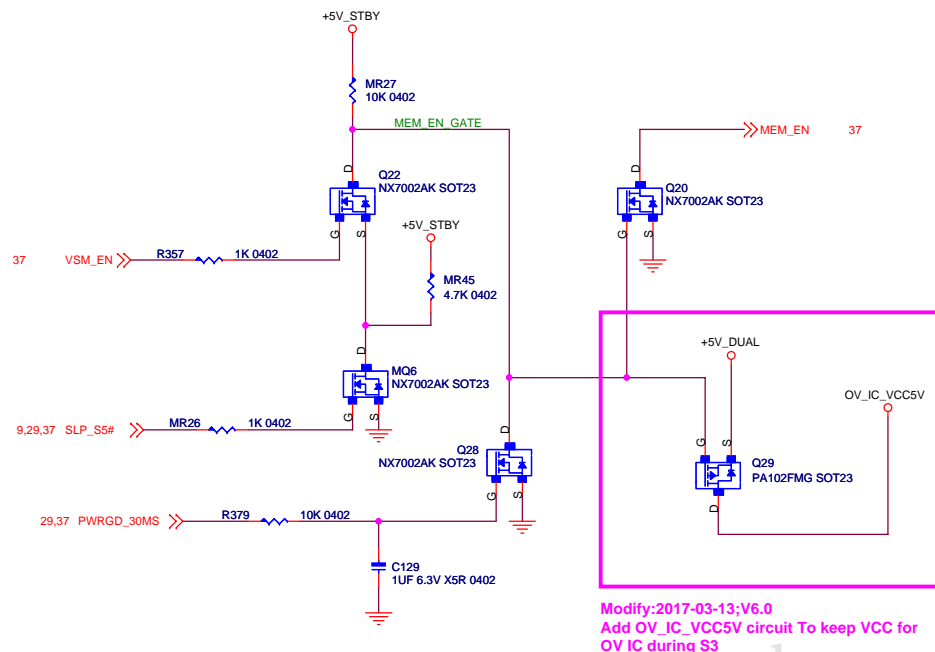
MT
Micro ATX(240*220)



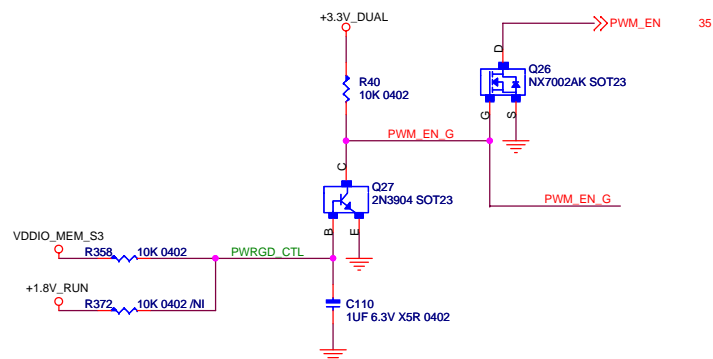
EMI SOLUTION



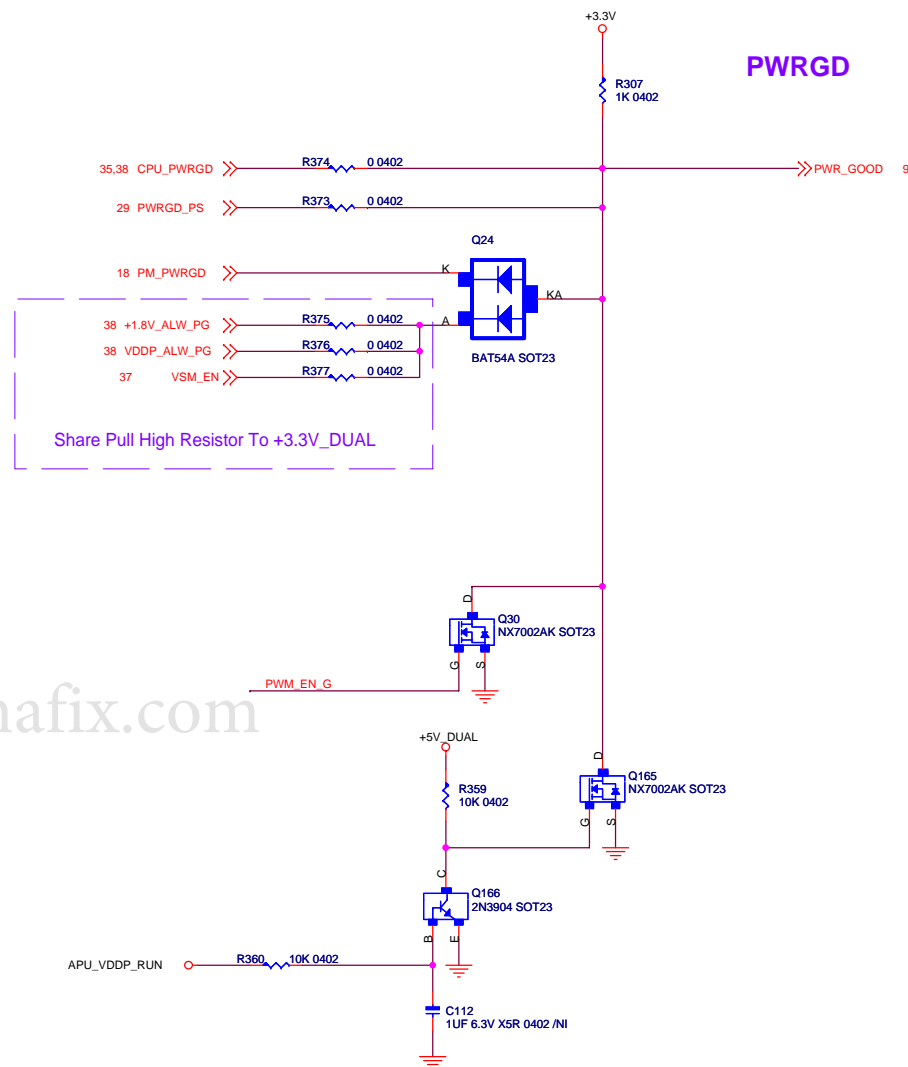
MEM POWER ENABLE



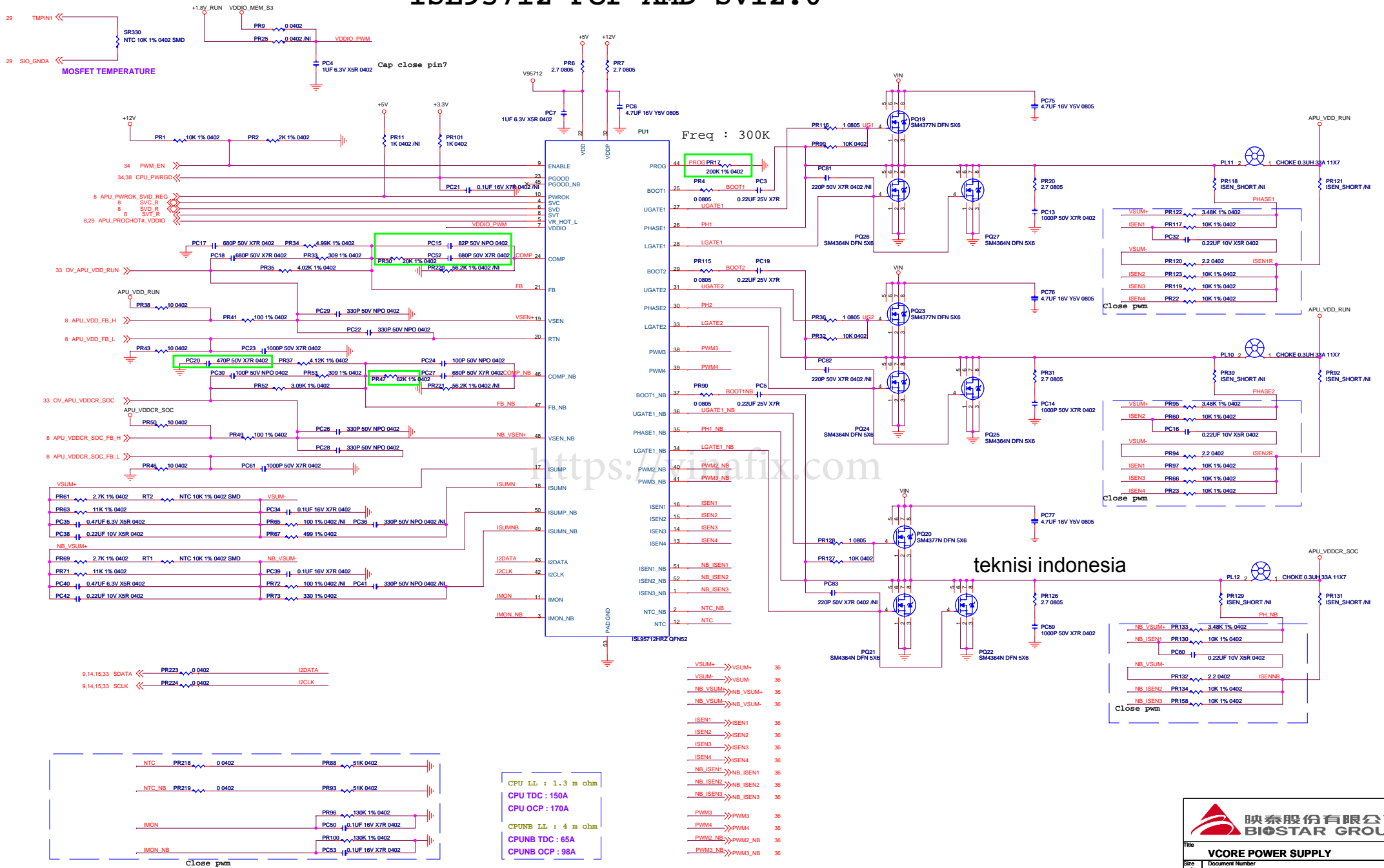
CPU PWM ENABLE



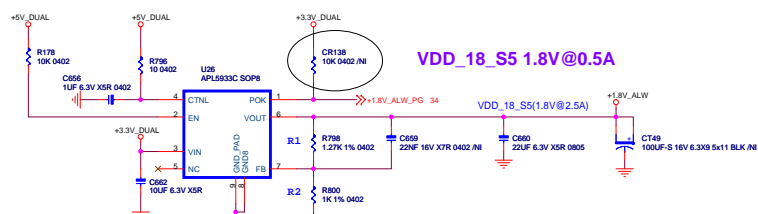
PWRGD



ISL95712 For AMD SVI2.0

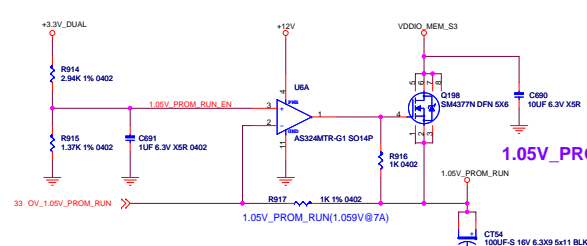
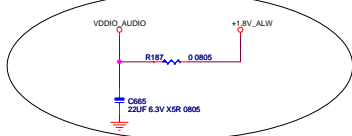




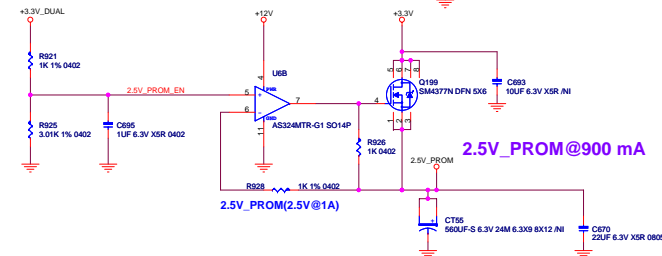


$$V_{out} = V_{ref}(0.8V) \times (R1/R2 + 1) = 1.816V @ 0.5A$$

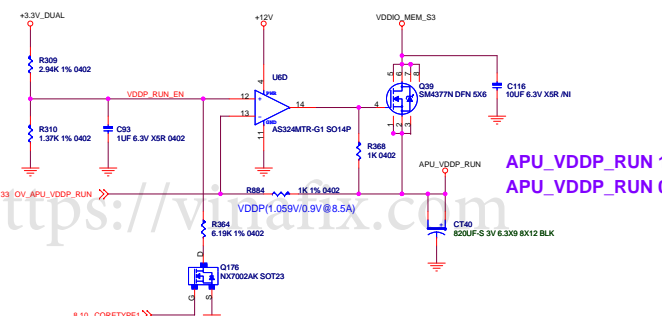
VDDIO_AUDIO 1.516V@0.25A



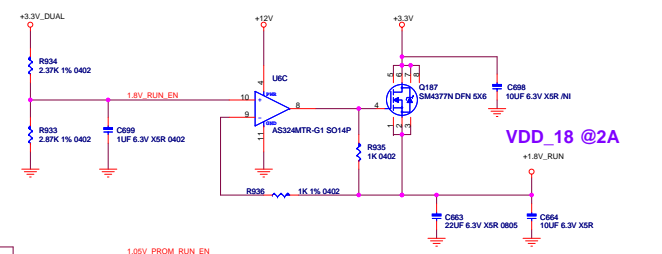
1.05V_PROM_RUN@5.5A



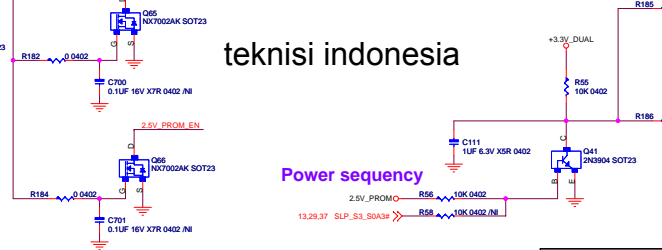
2.5V_PROM@900 mA



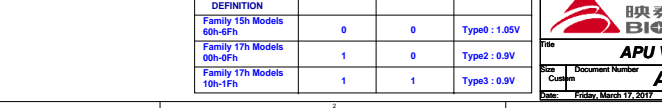
1.05V_PROM_S5 1.065V@50 mA



VDDP_ALW 1.062V@1A
VDDP_ALW 0.920V@1A



VDD_18 @2A



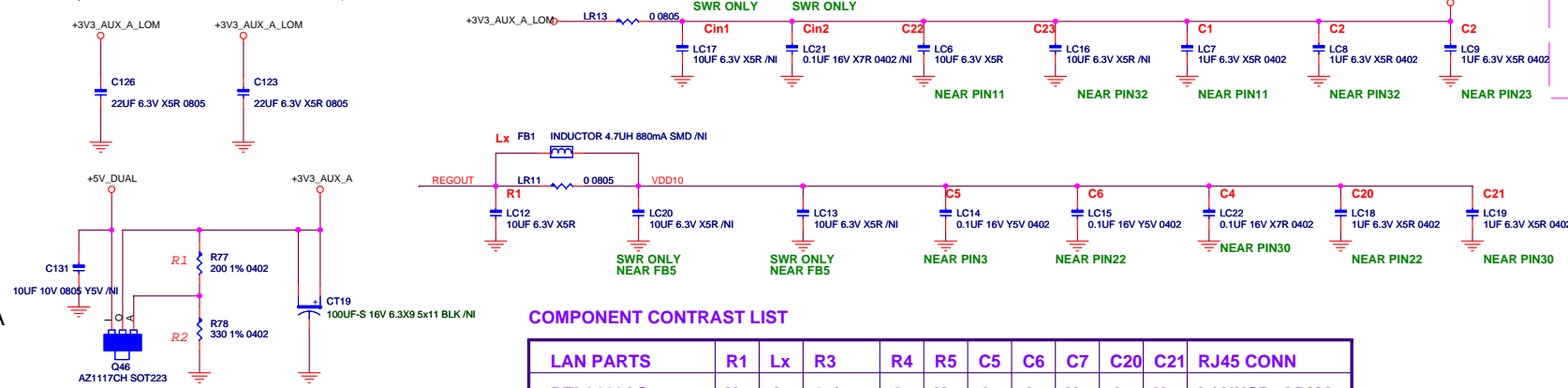
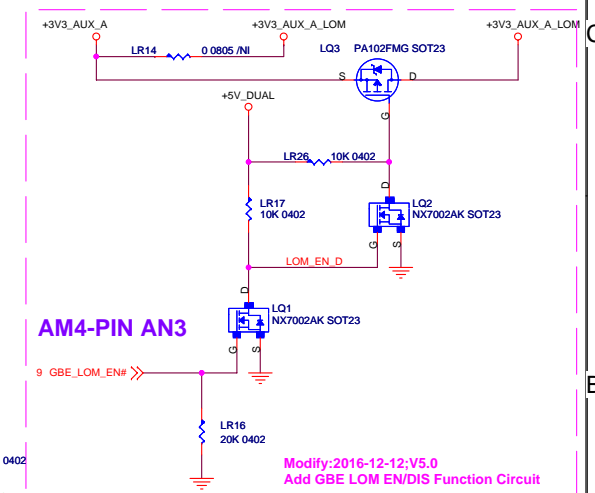
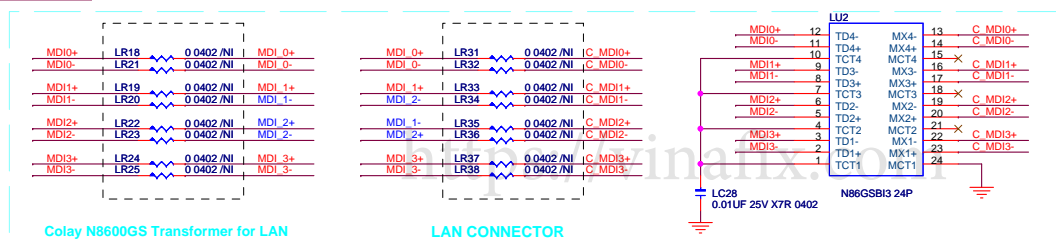
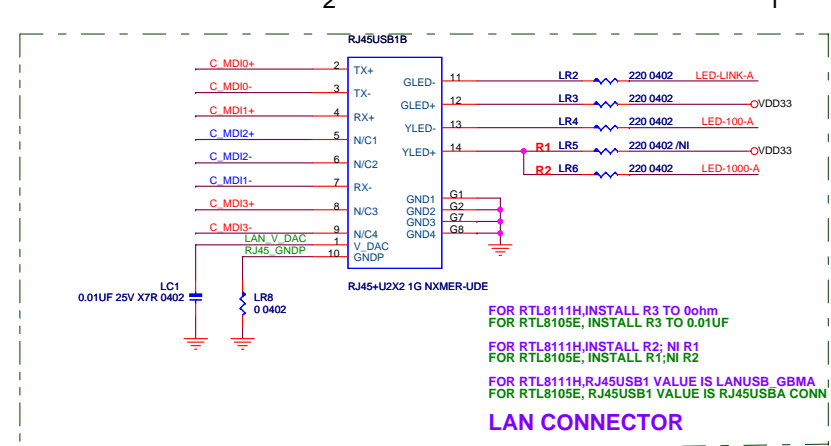
$$V_{out} = V_{ref}(0.8V) \times (R1/R2 + 1) = 3.332V @ 2A$$

teknisi indonesia

Power sequency

CORETYPE DEFINITION	CORETYPE 1	CORETYPE 0	
Family 15h Models 60h-6Fh	0	0	Type0 : 1.05V
Family 17h Models 60h-6Fh	1	0	Type2 : 0.9V
Family 17h Models 10h-1Fh	1	1	Type3 : 0.9V

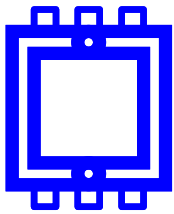
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COMPONENT CONTRAST LIST											
LAN PARTS	R1	Lx	R3	R4	R5	C5	C6	C7	C20	C21	RJ45 CONN
RTL8118AS	X	O	0ohm	O	X	O	O	X	O	X	LANUSB_GBMA
RTL8106E	O	X	0.01uF	X	O	X	X	O	X	O	RJ45USBA CONN

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Title LAN RTL8111H/8107E			
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(CPU1)



AM4RM-PC

(BAT1)



3V BATTERY SONY



JCMOS1(1_2)
JUMPER 2P B

(Y2)



X'TAL WIRE

(YY3)



X'TAL WIRE /NI

LB1



L-XXX V6.0 /NI

58-TB350BTC60-01

LABEL "TB350-BTC VER:6.0" 44x5.5mm/Silver

58-TA320BTC60-01

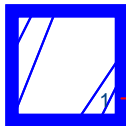
LABEL "TA320-BTC VER:6.0" 44x5.5mm/Silver

(SPI1)



W25Q128F QUAD SOIC8

FCH_HEATSINK



SBHS-AB35B-A4S /NI

FOR NETIN

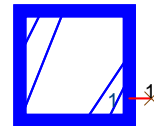
(FCH1)



SBHS-AB35B-A4S

FOR BOM

MOSHEATSINK



MOSHS-IZ17A

<https://vinafix.com> 20-120-544008H11

20-120-228201H1

20-120-544008H11 HEATSINK 54.4x40.5x10.9mm/BLACK/H1-NB696-HS07/.HOTEK
20-120-228201H1 MOS HEATSINK 22.4x82.7x24.5mm/BLACK/0288-0248F/.KG

PCB



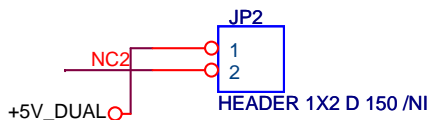
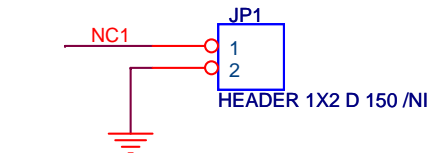
AB35B-A4S V6.0

98-AB35BA4S-R01P-060
86-AB35BA4S-R01P-060
96-AB35BA4S-R01P-060

15-Z78-106060RS AB35B-A4S VER:0.6 /OSP/BLACK/(210.00*295.00*1.5)mm/4L /ISUHN

98-AA32BA4S-R01P-060
86-AA32BA4S-R01P-060
96-AA32BA4S-R01P-060

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A

Document Number

AB35B-A4S

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6.0

Date: Friday, March 17, 2017


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- AB35B-A4S-V6.0 ChangeList 2017-03-14
- Based On AB35B-A4S-VER060
- 1.Page13:Update HDT_PWR Cirucit For Summit CPU +1.8V_RUN Leakage issue
 - 2.Modify Layout for DIMM slots remove 40mils to right side for CPU FAN mechanism Issue
 - 3.Page12/29:Add CPU Socket Occupied Function
 - 4.Page33/34:Add OV_IC_VCC5V circuit to keep VCC for OV IC during S3
 - 5.Page09/13:Update SLP_S3_S0 circuit For New request

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